- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

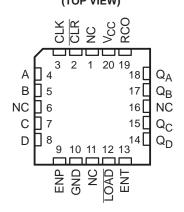
These synchronous, presettable, 4-bit decade and binary counters feature an internal carry look-ahead circuitry for application in high-speed counting designs. The SN54ALS162B is a 4-bit decade counter. The 'ALS161B, 'ALS163B, 'AS161, and 'AS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; they may be preset to any number between 0 and 9 or 15. Because presetting is synchronous, setting up a low level at the load (\overline{LOAD}) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163...J PACKAGE SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163...D OR N PACKAGE (TOP VIEW)

CLR [CLK [A [B [2 3	σ	16 15 14 13] V _{CC}] RCO] Q _A] Q _B
с[5		12	
D [11] Q _D
	7		10] ENT
GND [8		9] LOAD
				I

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The clear function for the 'ALS161B and 'AS161 is asynchronous. A low level at the clear (CLR) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, LOAD, or enable inputs. The clear function for the SN54ALS162B, 'ALS163B, and 'AS163 is synchronous, and a low level at CLR sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to CLR to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP and ENT inputs and a ripple-carry (RCO) output are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). The high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

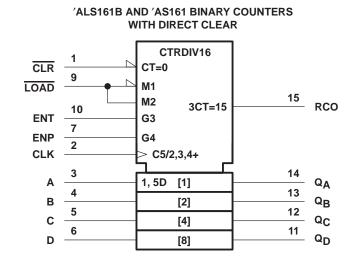
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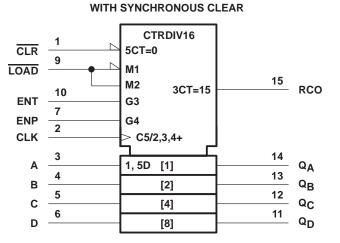
description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or LOAD) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

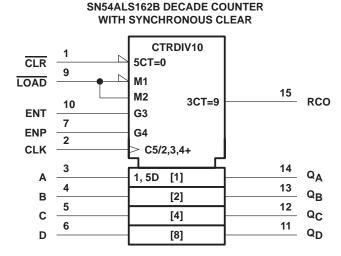
The SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, and SN54AS163 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS161B, SN74ALS163B, SN74AS161, and SN74AS163 are characterized for operation from 0°C to 70°C.

logic symbols[†]



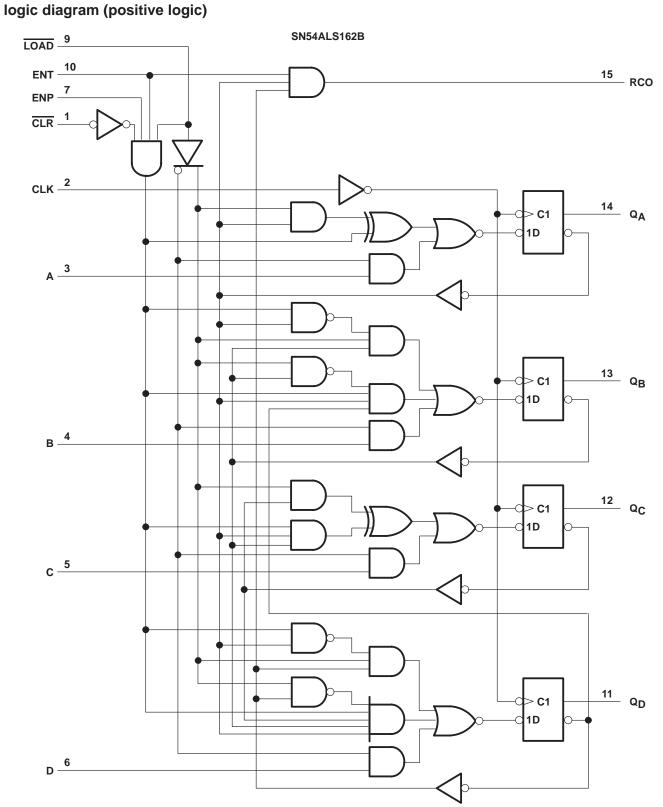


'ALS163B AND 'AS163 BINARY COUNTERS



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

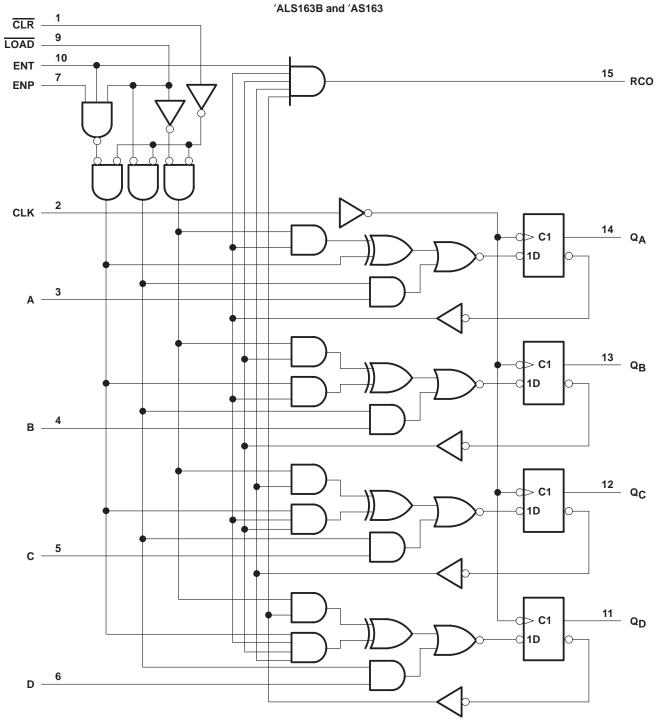




Pin numbers shown are for the J package.



logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages. 'ALS161B and 'AS161 synchronous binary counters are similar; however, CLR is asynchronous.

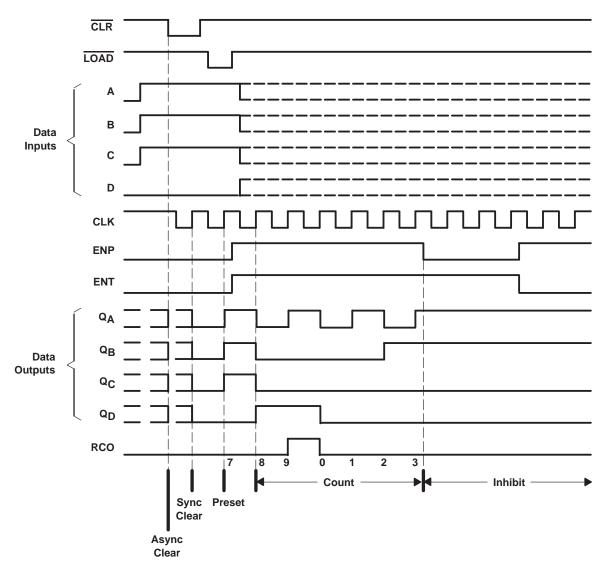


typical clear, preset, count, and inhibit sequences

SN54ALS162B

The following sequence is illustrated below:

- 1. Clear outputs to zero (SN54ALS162B is synchronous)
- 2. Preset to BCD 7
- 3. Count to 8, 9, 0, 1, 2, and 3
- 4. Inhibit



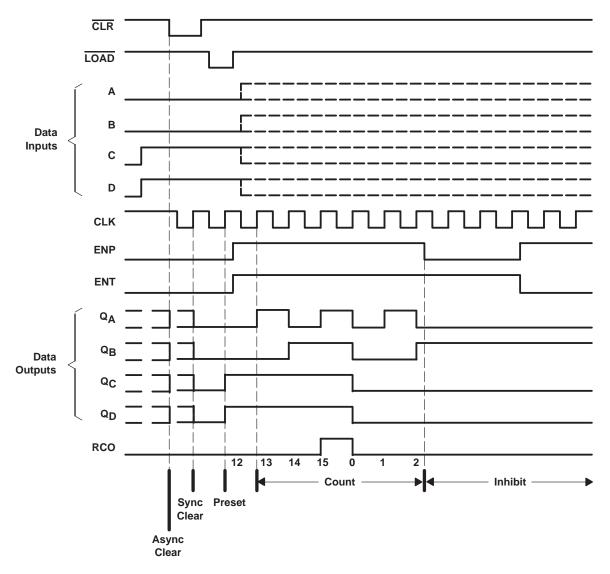


typical clear, preset, count, and inhibit sequences

'ALS161B, 'AS161, 'ALS163B, and 'AS163

The following sequence is illustrated below:

- 1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous.)
- 2. Preset to binary 12
- 3. Count to 13, 14, 15, 0, 1, and 2
- 4. Inhibit





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	
Dperating free-air temperature range, T _A : SN54ALS161B, SN54ALS162B, SN54ALS163B	2
torage temperature range	2

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

				SNS	54ALS16 54ALS16 54ALS16	2B	SN74ALS161B SN74ALS163B		UNIT		
				MIN	NOM	MAX	MIN	NOM MAX			
VCC	Supply voltage			4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input vol	High-level input voltage					2			V	
VIL	Low-level input volt	tage				0.7			0.8	V	
IOH	High-level output current					-0.4			-0.4	mA	
IOL	Low-level output cu	r-level output current				4			8	mA	
fclock	Clock frequency		0		22	0		40	MHz		
÷	Dulas duration	CLR high or low		20			12.5				
tw	Pulse duration 'ALS161B	CLR low	20			15			ns		
		A, B, C, D		50			15				
		LOAD		20			15				
		'ALS161B		25			15				
t _{su}	Setup time before CLK↑	SN54ALS162B, 'ALS163B	ENP, ENT	20			15			ns	
	Delore OLICI	'ALS161B	CLR inactive	10			10				
			CLR low	20			15				
	SIN34ALS162B	SN54ALS162B, 'ALS163B	CLR high	20			10				
th	Hold time, all synch	nronous inputs after CLK1	-	0			0			ns	
Тд	Operating free-air t	emperature		-55		125	0		70	°C	



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN5	SN54ALS161B SN54ALS162B SN54ALS163B			SN74ALS161B SN74ALS163B		
				TYP†	MAX	MIN	TYP†	MAX	
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.5			-1.5	V
Vон	V _{CC} = 4.5 V to 5.5 V,	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		V
Ve		I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$	I _{OL} = 8 mA					0.35	0.5	v
lj	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
IIH	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
IIL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
IO‡	V _{CC} = 5.5 V,	V _O = 2.25 V	-20		-112	-30		-112	mA
ICC	V _{CC} = 5.5 V			12	21		12	21	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. [‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V(Cl Rl T <i>f</i>	UNIT			
			SN54AL	S161B	SN74AL	S161B	
			MIN	MAX	MIN	MAX	
fmax			22		40		MHz
^t PLH	CLK	RCO	5	34	5	20	ns
^t PHL	ULK	RCO	5	27	5	20	115
^t PLH	CLK	Any O	4	19	4	15	20
^t PHL	ULK	Any Q	6	25	6	20	ns
^t PLH	ENT	RCO	3	18	3	13	20
^t PHL	ENT	RCU	3	17	3	13	ns
t	CLR Any Q RCO	8	27	8	24		
^t PHL		RCO	11	32	11	23	ns

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



switching characteristics (see Figure 3)

PARAMETER	FROM	то	CL RI	= 50 pF = 500 Ω	V to 5.5 V ; 2, o MAX [†]	3	UNIT
	(INPUT)	(OUTPUT)	(OUTPUT) SN54ALS162B SN54ALS163B SN74ALS163B		1		
			MIN	MAX	MIN	MAX	
f _{max}			35		40		MHz
^t PLH	CLK	RCO	5	25	5	20	ns
^t PHL	ULK	KCO	5	25	5	20	115
^t PLH	CLK	Any Q	4	18	4	15	ns
^t PHL			6	25	6	20	115
^t PLH	ENT	RCO	3	16	3	13	ns
^t PHL		NOU	3	16	3	13	115

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V _{CC}	7 V
Input voltage, V _I	
Operating free-air temperature range, T _A : SN54AS161, SN54AS163	-55°C to 125°C
SN74AS161, SN74AS163	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

				-	N54AS16		-	SN74AS161 SN74AS163		UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	ply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input vol	tage		2			2			V
VIL	Low-level input volt	age				0.8			0.8	V
ЮН	High-level output c	urrent				-2			-2	mA
IOL	Low-level output current					20			20	mA
fclock*	Clock frequency					65	0		75	MHz
د *	Pulse duration CLR high 'AS161	CLR high or low		7.7			6.7			
t _w *		'AS161	CLR low	10			8			ns
		A, B, C, D		10			8			
		LOAD		10			8			
.	Setup time	ENP, ENT		10			8			
t _{su} *	before CLK↑	'AS161	CLR inactive	10			8			ns
		(4.0.4.0.)	CLR low	14			12			
		'AS163	CLR high (inactive)	10			9			
t _h *	Hold time, all synchronous inputs after CLK↑		2			0			ns	
ТА	Operating free-air t	emperature		-55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CO	TEST CONDITIONS		SN54AS161 SN54AS163			SN74AS161 SN74AS163		
				MIN	түр†	YP [†] MAX MIN TYP [†] MAX		MAX		
VIK		V _{CC} = 4.5 V,	II = -18 mA			-1.2			-1.2	V
VOH		V _{CC} = 4.5 V to 5.5 V,	$I_{OH} = -2 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		V
VOL		V _{CC} = 4.5 V,	I _{OL} = 20 mA		0.25	0.5		0.25	0.5	V
	LOAD					0.3			0.3	
lj –	ENT	V _{CC} = 5.5 V,	V ₁ = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
	LOAD					60			60	
Чн	ENT	V _{CC} = 5.5 V,	V _I = 2.7 V	= 2.7 V 40				40	μA	
	All others	7				20			20	
	LOAD					-1.5			-1.5	
Ι _Ι Γ	ENT	V _{CC} = 5.5 V,	$V_I = 0.4 V$			-1			-1	mA
	All others					-0.5			-0.5	
10‡		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA
ICC		V _{CC} = 5.5 V			35	53		35	53	mA

[†] All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristics (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL RL	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				
			SN54A	AS161	SN74A	S161		
			MIN	MAX	MIN	MAX		
^f max*			65		75		MHz	
		RCO (with LOAD high)	1	8.5	1	8		
^t PLH	CLK	CLK RCO (with LOAD low)	RCO (with LOAD low)	3	17.5	3	16.5	ns
^t PHL		RCO	2	14	2	12.5		
^t PLH	CLK	AmirO	1	7.5	1	7		
^t PHL	CLK	Any Q	2	14	2	13	ns	
^t PLH		DCO.	1.5	10	1.5	9		
^t PHL	ENT	RCO	1	9.5	1	8.5	ns	
	CLR	Any Q	2	14	2	13		
^t PHL	ULR	RCO	2	14	2	12.5	ns	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested. § For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



switching characteristics (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX [†]			
			SN54	AS163	SN74A	S163	
			MIN	MAX	MIN	MAX	
f _{max} *			65		75		MHz
t		RCO (with LOAD high)	1	8.5	1	8	
^t PLH	CLK	RCO (with LOAD low)	3	17.5	3	16.5	ns
^t PHL		RCO	2	14	2	12.5	
^t PLH	CLK	Any Q	1	7.5	1	7	ns
^t PHL		Any Q	2	14	2	13	115
^t PLH	ENT	RCO	1.5	10	1.5	9	ns
^t PHL		RCO	1	9.5	1	8.5	115

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

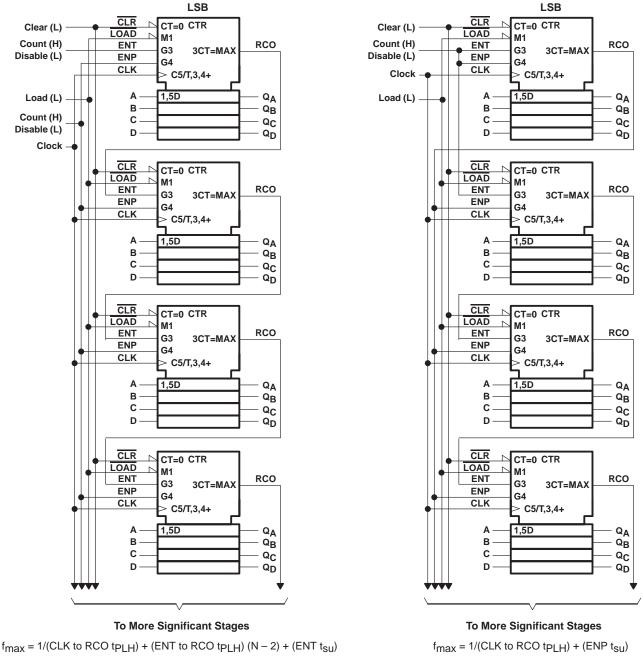


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APPLICATION INFORMATION

n-bit synchronous counters

This application demonstrates how the ripple-mode carry circuit (see Figure 1) and the carry-look-ahead circuit (see Figure 2) can be used to implement a high-speed n-bit counter. The SN54ALS162B counts in BCD. The 'ALS161B, 'AS161, 'ALS163B, and 'AS163 count in binary. When additional stages are added, the f_{max} decreases in Figure 1, but remains unchanged in Figure 2.

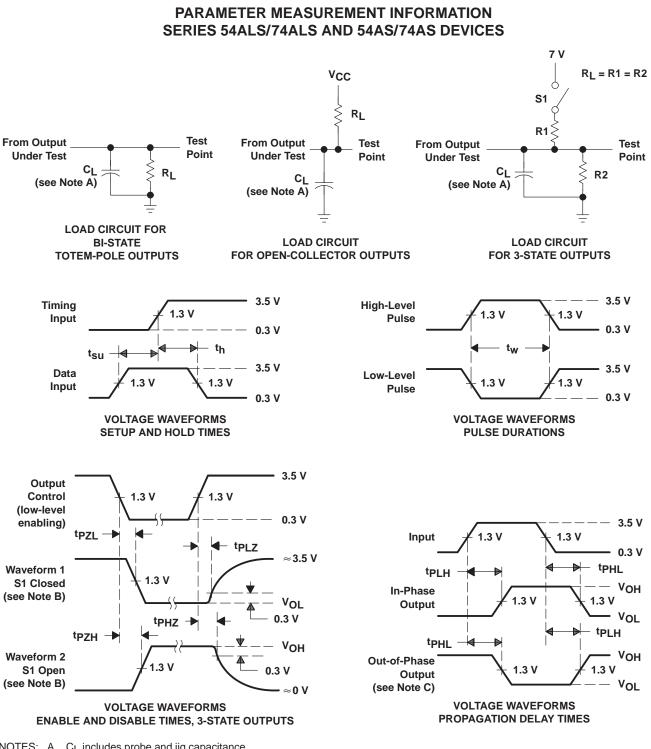








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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- All input pulses have the following characteristics: PRR \leq 1 MHz, t_f = t_f = 2 ns, duty cycle = 50%. D
- E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms



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