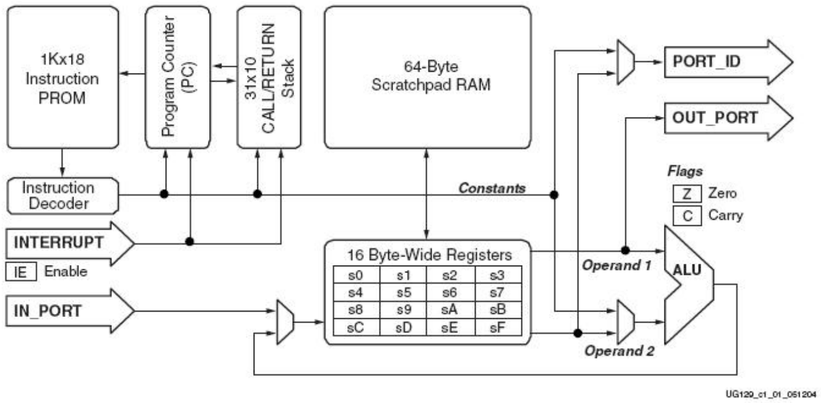



*Figure 1-1:* **PicoBlaze Embedded Microcontroller Block Diagram**

*Table 8-1:* **PicoBlaze Performance Using Slowest Speed Grade**

| FPGA Family (Speed Grade) | Maximum Clock Frequency | Maximum Execution Performance |
|---|---|---|
| Spartan-3 (-4) FPGA | 88 MHz | 44 MIPS |
| Virtex-II (-6) FPGA | 152 MHz | 76 MIPS |
| Virtex-II Pro (-7) FPGA | 200 MHz | 100 MIPS |

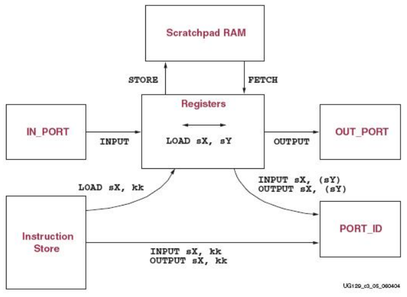
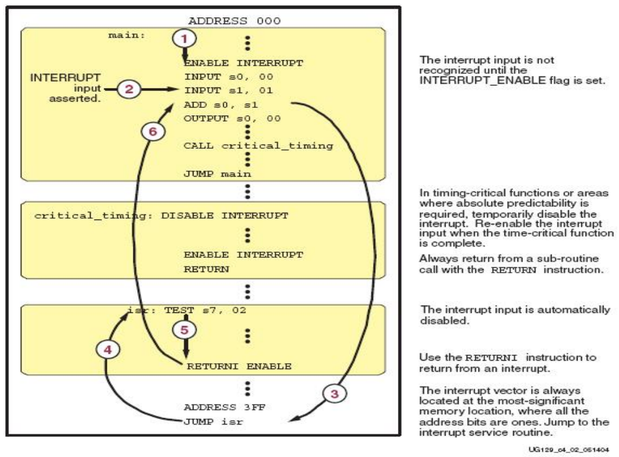



*Figure 3-26:* **Data Movement Instructions**

## PicoBlaze Instruction Set*

| Program Control | Logical | Arithmetic |
|---|---|---|
| JUMP aaa | LOAD sX,kk | ADD sX,kk |
| JUMP Z,aaa | AND sX,kk | ADDCY sX,kk |
| JUMP NZ,aaa | OR sX,kk | SUB sX,kk |
| JUMP C,aaa | XOR sX,kk | SUBCY sX,kk |
| JUMP NC,aaa | TEST sX,kk | COMPARE sX,kk |
| | LOAD sX,sY | ADD sX,sY |
| | AND sX,sY | ADDCY sX,sY |
| CALL aaa | OR sX,sY | SUB sX,sY |
| CALL Z,aaa | XOR sX,sY | SUBCY sX,sY |
| CALL NZ,aaa | TEST sX,sY | COMPARE sX,sY |
| CALL C,aaa | | |
| CALL NC,aaa | **Shift and Rotate** | **Storage** |
| | SR0 sX | FETCH sX,ss |
| RETURN | SR1 sX | FETCH sX,(sY) |
| RETURN Z | SRX sX | STORE sX,ss |
| RETURN NZ | SRA sX | STORE sX,(sY) |
| RETURN C | RR sX | |
| RETURN NC | SL0 sX | **Interrupt** |
| | SL1 sX | RETURNI ENABLE |
| **Input/Output** | SLX sX | RETURNI DISABLE |
| INPUT sX,pp | SLA sX | ENABLE INTERRUPT |
| INPUT sX,(sY) | RL sX | DISABLE INTERRUPT |
| OUTPUT sX,pp | | *All instructions execute in 2 clock cycles* |
| OUTPUT sX,(sY) | | |




The interrupt input is not recognized until the INTERRUPT_ENABLE flag is set.

In timing-critical functions or areas where absolute predictability is required, temporarily disable the interrupt. Re-enable the interrupt input when the time-critical function is complete.

Always return from a sub-routine call with the `RETURN` instruction.

The interrupt input is automatically disabled.

Use the `RETURNI` instruction to return from an interrupt.

The interrupt vector is always located at the most-significant memory location, where all the address bits are ones. Jump to the interrupt service routine.

*Figure 4-2:* **Example Interrupt Flow**

# PicoBlaze™ softcore processor

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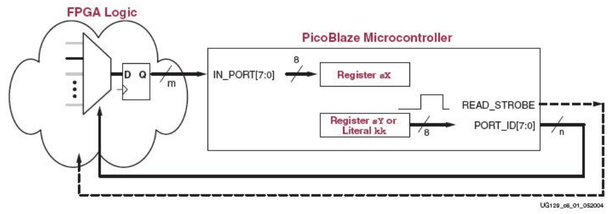


*Figure 6-1:* **INPUT Operation and FPGA Interface Logic**

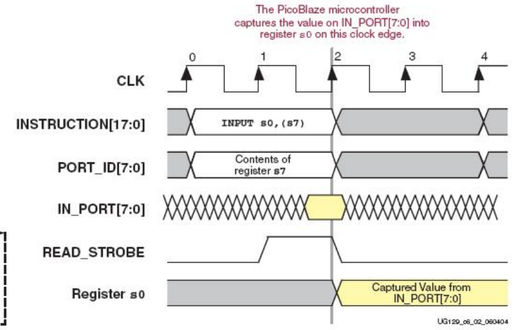


*Figure 6-2:* **Port Timing for INPUT Instruction**

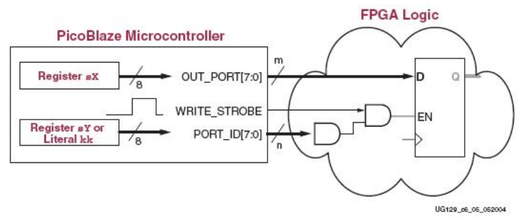


*Figure 6-5:* **OUTPUT Operation and FPGA Interface**

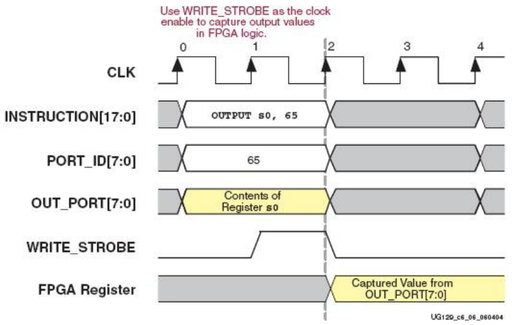


*Figure 6-6:* **Port Timing for OUTPUT Instruction**

*Table 10-1:* **PicoBlaze Development Environments**

| | Xilinx KCPSM3 | Mediatronix pBlazIDE | Xilinx System Generator |
|---|---|---|---|
| Platform Support | Windows | Windows 98, Windows 2000, Windows NT, Windows ME, Windows XP | Windows 2000, Windows XP |
| Assembler | Command-line in DOS window | Graphical | Command-line within System Generator |
| Instruction Syntax | KCPSM3 | PBlazIDE | KCPSM3 |
| Instruction Set Simulator | Facilities provided for VHDL simulation | Graphical/Interactive | Graphical/Interactive |
| Simulator Breakpoints | N/A | Yes | Yes |
| Register Viewer | N/A | Yes | Yes |
| Memory Viewer | N/A | Yes | Yes |