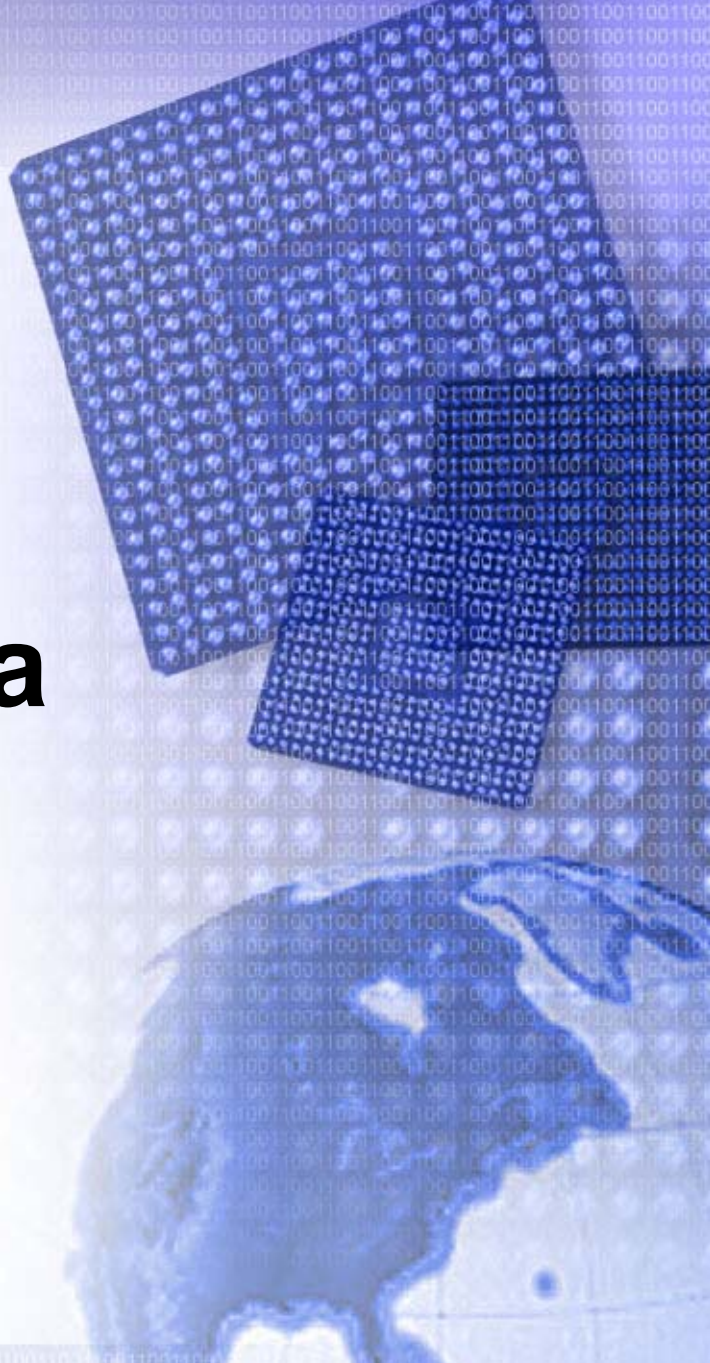
XILINX®

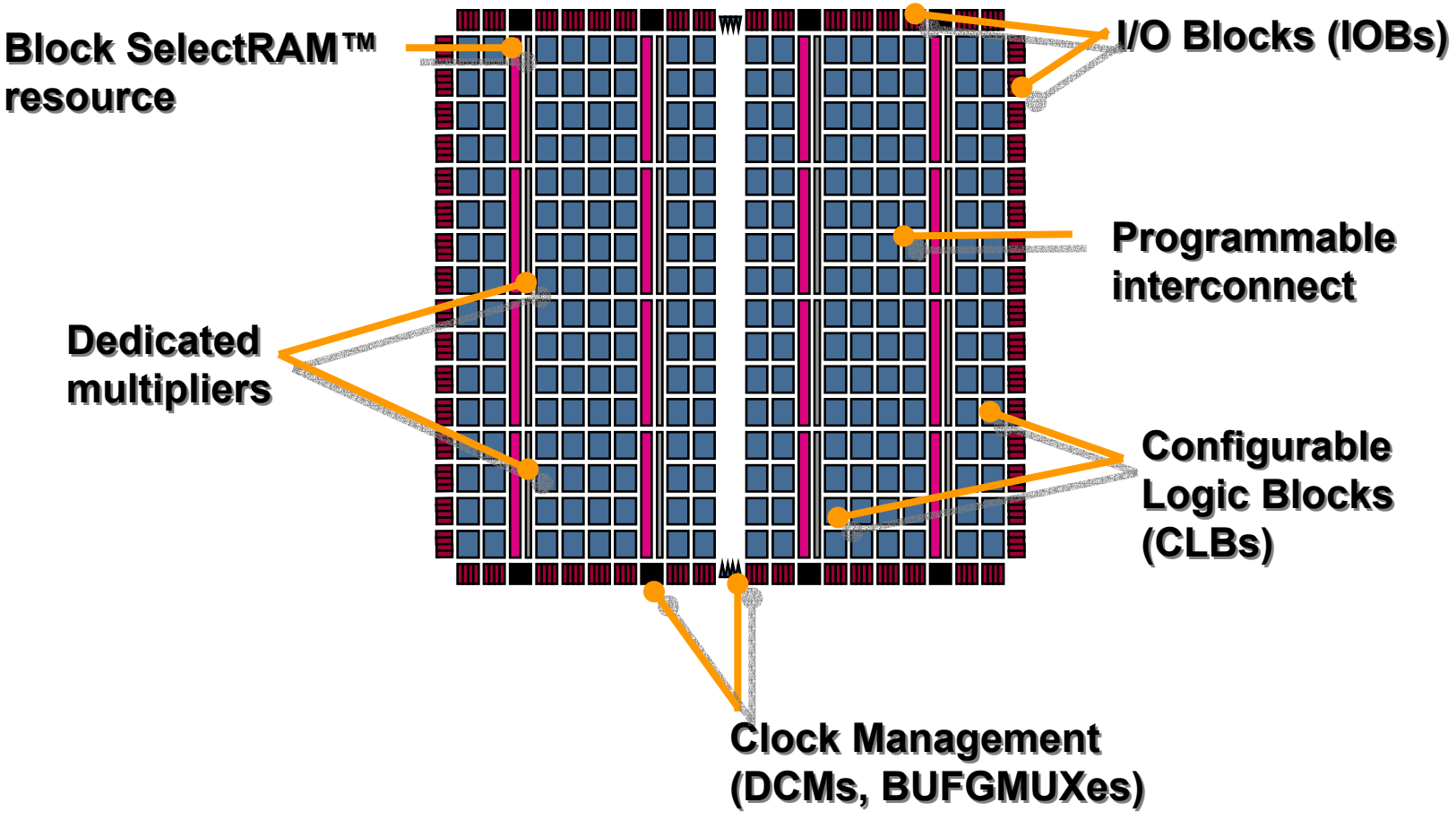


Arquitectura de una FPGAs de Xilinx

Una Vista por encima

- Todas las FPGAs Xilinx contienen en general los mismos recursos básicos
  - Slices (agrupados dentro de los CLBs)
    - Contiene registros y lógica combinacional
  - Bloques I/O o IOBs
    - Interfase entre la FPGA y el mundo exterior
  - Interconexión programable
  - Otros Recursos
    - Memoria
    - Multiplicadores
    - Buffer para relojes globales
    - Boundary scan logic

Arquitectura de la Spartan 3



Xilinx Spartan-3 Family

- Programmable Input Output Blocks (IOB).
- Clock Management Blocks (DCM).
- Configurable Logic Blocks (CLB).
- Flexible Synchronous Memory (BlockRAM).
- A variety of programmable routing resources.

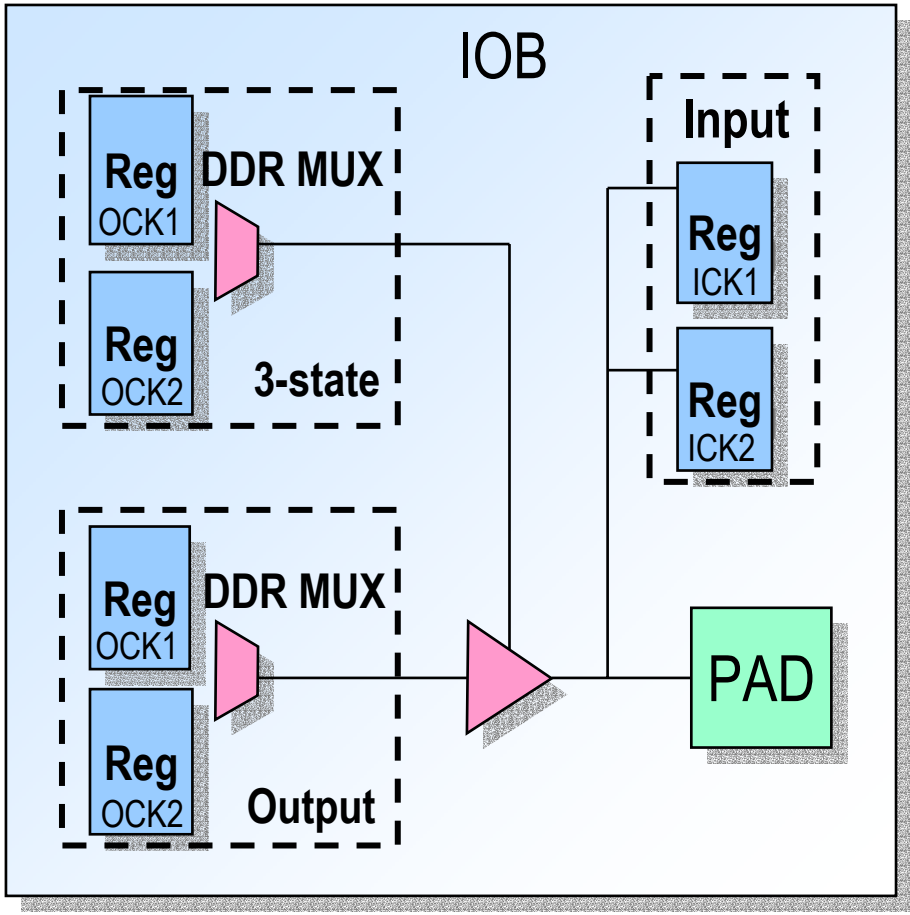
IOB Element

Input path
- Two DDR registers

Output path
- Two DDR registers
- Two 3-state enable DDR registers

Separate clocks and clock enables for I and O

Set and reset signals are shared



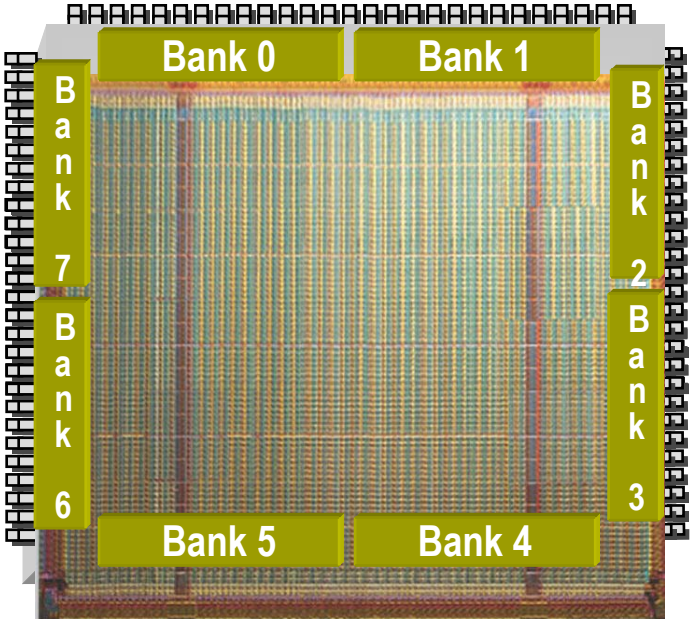
SelectIO Standard

- Allows direct connections to external signals of varied voltages and thresholds
  - Optimizes the speed/noise tradeoff
  - Saves having to place interface components onto your board
- Differential signaling standards
  - LVDS, BLVDS, ULVDS
  - LDT
  - LVPECL

SelectIO Standard

- Single-ended I/O standards
  - LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
  - PCI-X at 133 MHz, PCI (3.3V at 33 MHz and 66 MHz)
  - GTL, GTLP
  - and more!

Comprehensive Connectivity



- Single ended and differential.
  - 784 single-ended, 344 differential pairs.
  - 622 Mb/sec LVDS.
  - 24 I/O standards, 8 flexible I/O banks.
  - PCI 32/33 and 64/33 support.
  - Eliminate costly bus transceivers.
- 3.3V, 2.5V, 1.8V, 1.5V, 1.2V

Chip-to-Chip Interfacing: LVDS, LVCMOS, LVTTL

Backplane Interfacing: GTL, GTL+, PCI, BLVDS

High-speed Memory Interfacing: HSTL, SSTL

I/O Block Advantages

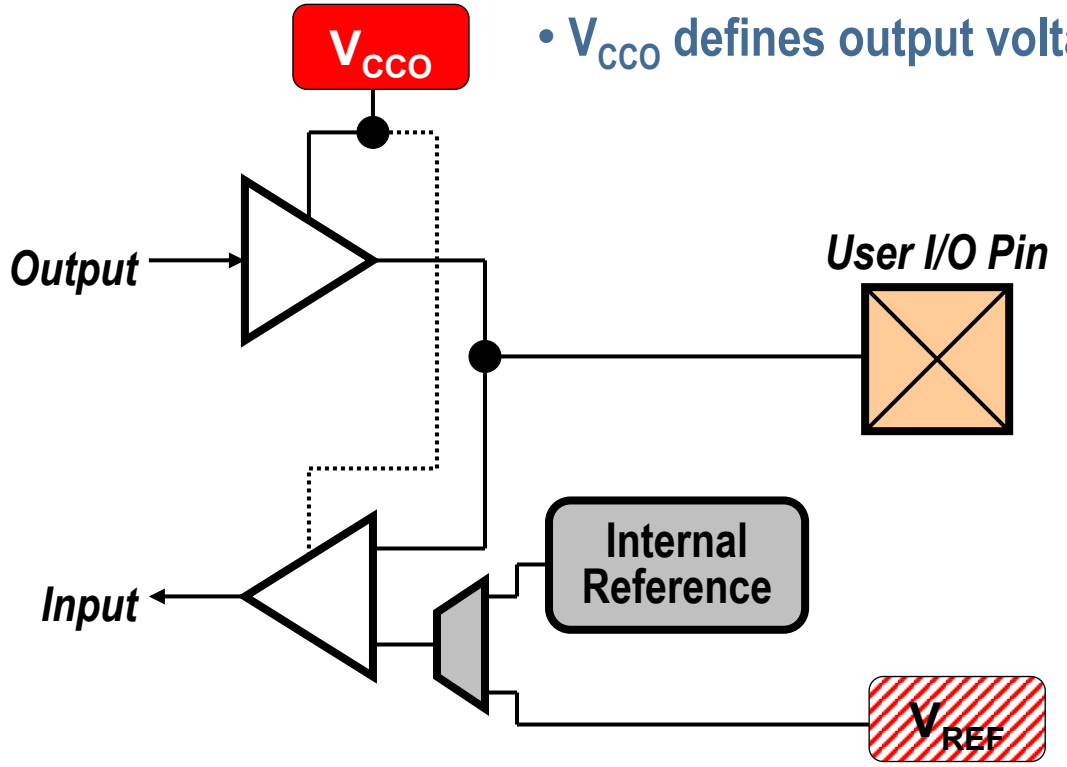
- Independent registers.
  - Fast bus operations.
  - Interface to high-speed memory like ZBT and QDR.
  - Increase system performance with fast Tsu and Tco.
- Lower ground bounce with slew rate control.
- Zero hold-time for registered input signals using programmable input delay.
- Lower power consumption with keeper circuit.

SelectIO

	Standard	Output V_{CCO}	Input V_{REF}
Single ended	LVTTL	3.3V	--
	LVCMOS33	3.3V	--
	LVCMOS25	2.5V	--
	LVCMOS18	1.8V	--
	LVCMOS15	1.5V	--
	LVCMOS12	1.2V	--
	PCI 32/64 bit 33MHz	3.3V	--
	SSTL2 Class I	2.5V	1.25V
	SSTL2 Class II	2.5V	1.25V
	SSTL18 Class I	1.8V	0.9V
	HSTL Class I	1.5V	0.75V
	HSTL Class III	1.5V	0.9V
	HSTL18 Class I	1.8V	0.9V
	HSTL18 Class II	1.8V	0.9V
	HSTL18 Class III	1.8V	1.1V
	GTL	--	0.8V
	GTL+	--	1.0V
Differential	LVDS2.5	2.5V	--
	Bus LVDS2.5	2.5V	--
	Ultra LVDS2.5	2.5V	--
	LVDS_ext2.5	2.5V	--
	RSDS	2.5V	--
	LDT2.5	2.5V	--

- More standards for system integration.
- Differential standards.
  - Higher I/O performance.
  - Lower power, lower cost.

SelectIO Standards



- V_{CCO} defines output voltage

- V_{REF} defines input threshold reference voltage
- Available as user I/O when using internal reference

SelectIO Output Banks

Each bank has an output driver voltage (V_{CCO}).

- Shared among all I/Os in that bank.
- All I/O in a bank must use the same voltage source.
- All V_{CCO} pins in a bank must be the same voltage.

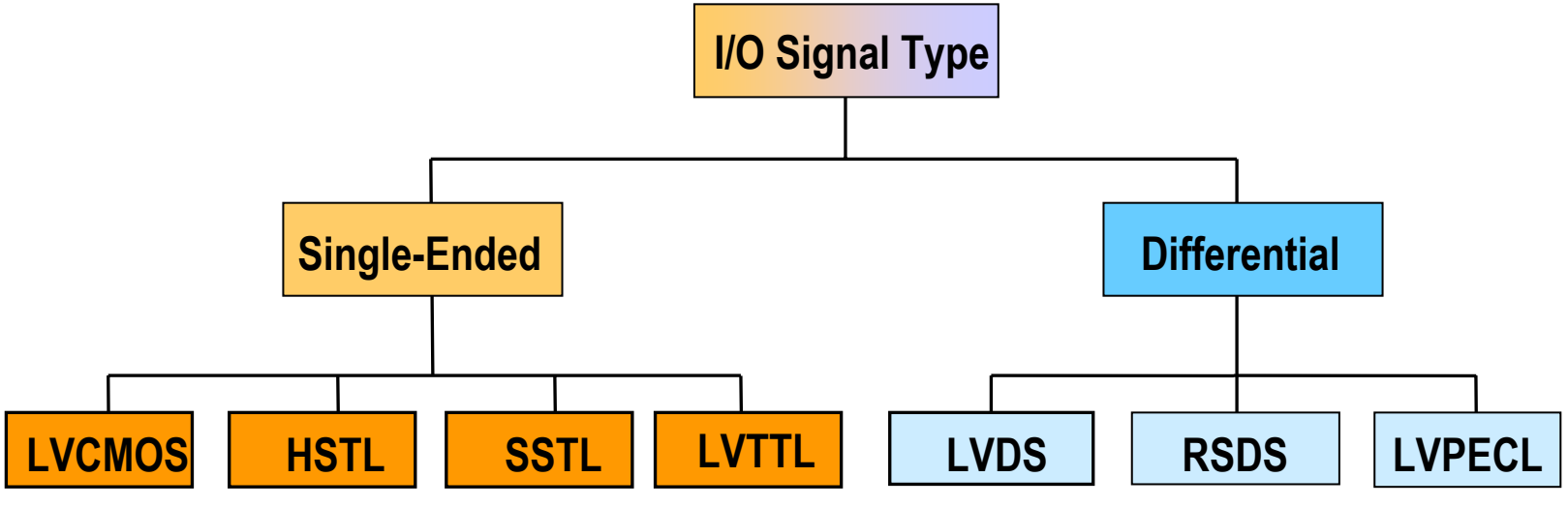
Only one V_{CCO} voltage for TQ144 per side.

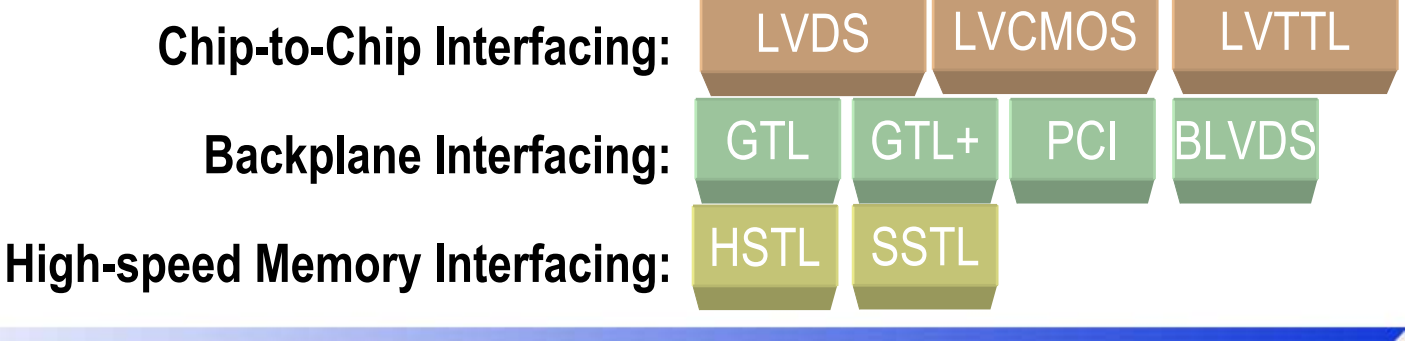
Outputs not requiring V_{CCO} fit in the bank.

SelectIO Input Banks

- Each bank has an input reference voltage (V_{REF}).
  - I/O in a bank must use the same reference voltage.
  - V_{REF} pins in a bank must be tied to the same voltage.
- Inputs not requiring a V_{REF} fit in the bank.
- V_{REF} pins in a bank available as additional I/O if I/O type does not require V_{REF}.

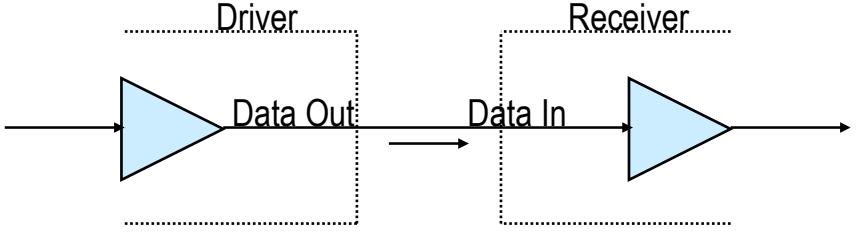
I/O Signal Types



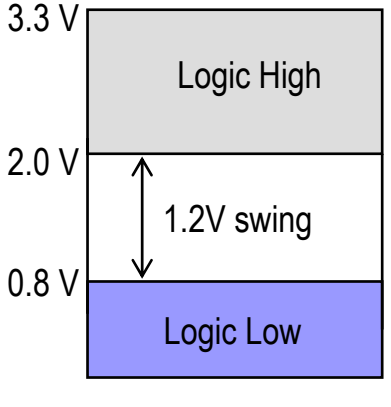


Single Ended I/O

- Traditional means of data transfer.
- Data is carried on a single line.
- Large voltage swing between logic levels.



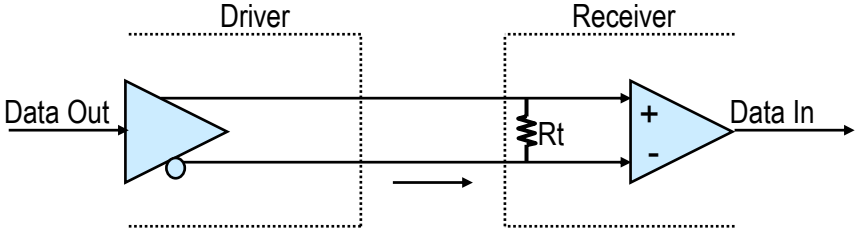
Single ended data transfer



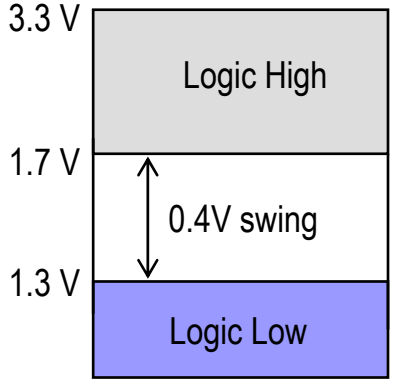
LVTTL input levels

Differential I/O

- One data bit is carried through two signal lines.
- Voltage difference determines logic level.
- Small voltage swing between logic levels.



Differential data transfer

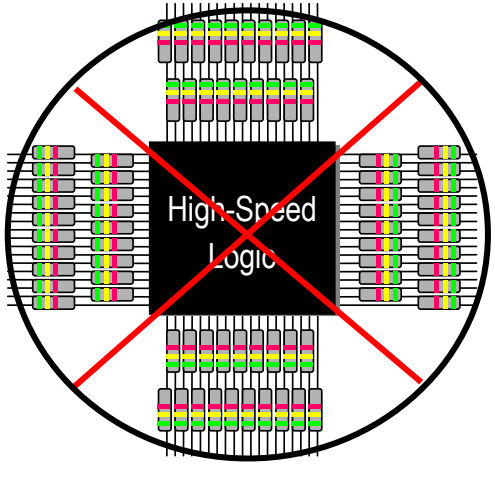


LVDS input levels

Differential I/O Benefits

- Small voltage swing between pairs.
  - Reduced emissions.
  - High performance per pin pair.
  - Reduced power consumption.
  - Improved noise rejection.
- Significant cost savings.
  - Fewer pins, board layers, board traces.
  - Smaller connectors.

Digitally Controlled Impedance Drivers



- On-chip I/O termination.
- Reduce total board cost.
  - Eliminate termination resistors.
  - Easier layout and fewer layers.
- Increases system reliability.
  - Greatly reduces component count.
  - Lower chance of failures.
- Elimination of stub reflection noise.
  - No traces between termination resistor and package pins.

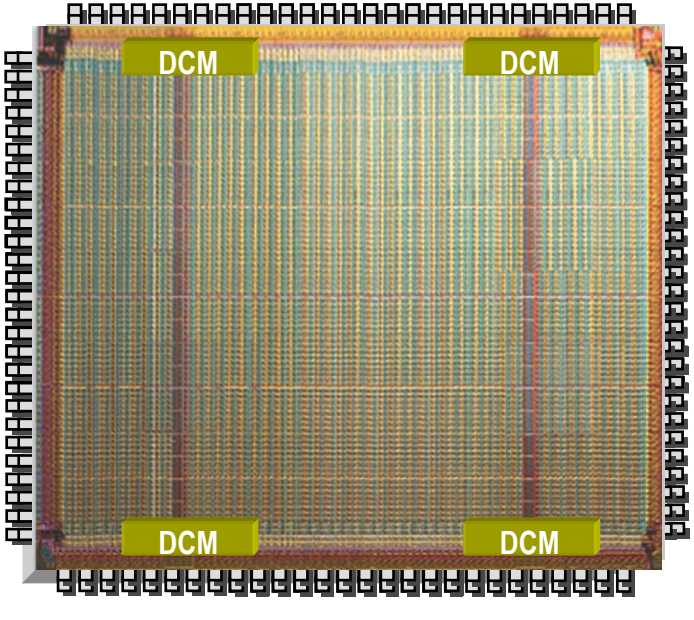
Digital Controlled Impedance (DCI)

- DCI provides
  - Output drivers that match the impedance of the traces
  - On-chip termination for receivers and transmitters
- DCI advantages
  - Improves signal integrity by eliminating stub reflections
  - Reduces board routing complexity and component count by eliminating external resistors
  - Eliminates the effects of temperature, voltage, and process variations by using an internal feedback circuit

Xilinx Spartan-3 Family

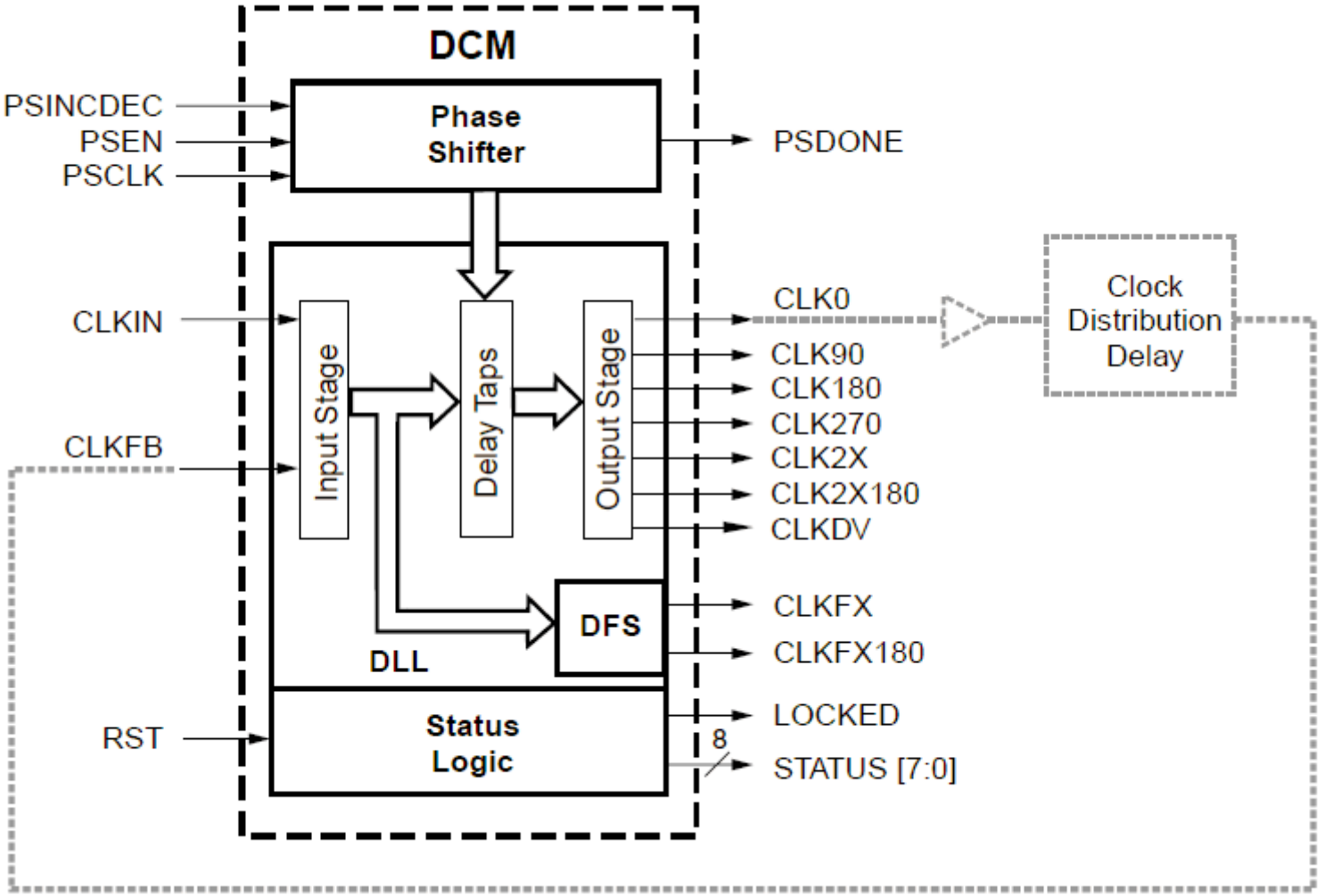
- Programmable Input Output Blocks (IOB).
- Clock Management Blocks (DCM).
- Configurable Logic Blocks (CLB).
- Flexible Synchronous Memory (BlockRAM).
- A variety of programmable routing resources.

Digital Clock Manager (DCM)



- Delay Locked Loop (DLL)
  - Clock phase de-skew.
  - 50% duty cycle correction.
  - 25 MHz to 280 MHz.
  - Simple phase shifts.
- Digital Phase Shift (DPS)
  - (Period / 256) increments.
- Digital Frequency Synthesis (DFS)
  - M/N clock multiply and divide.
  - M= 2 to 32, N= 1 to 32

DCM Functional Blocks



Clock Management Summary

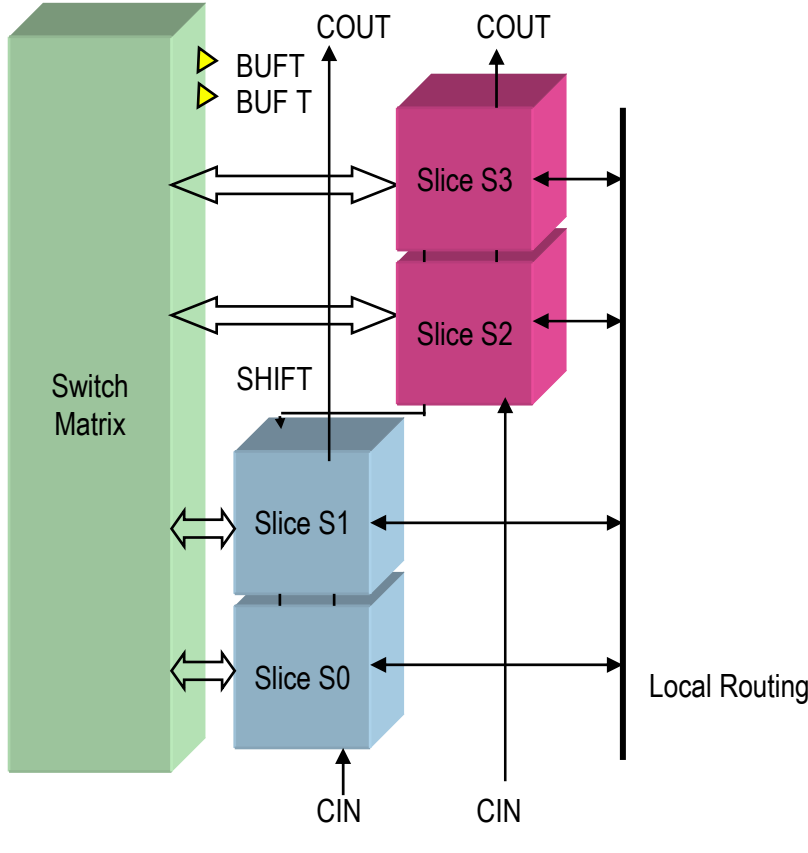
- All digital DLL implementation.
  - Clock deskew.
  - Input noise rejection.
  - 50/50 duty cycle correction.
  - Clock mirroring.
- Multiply or divide clock.
- Programmable phase shift.

Xilinx Spartan-3 Family

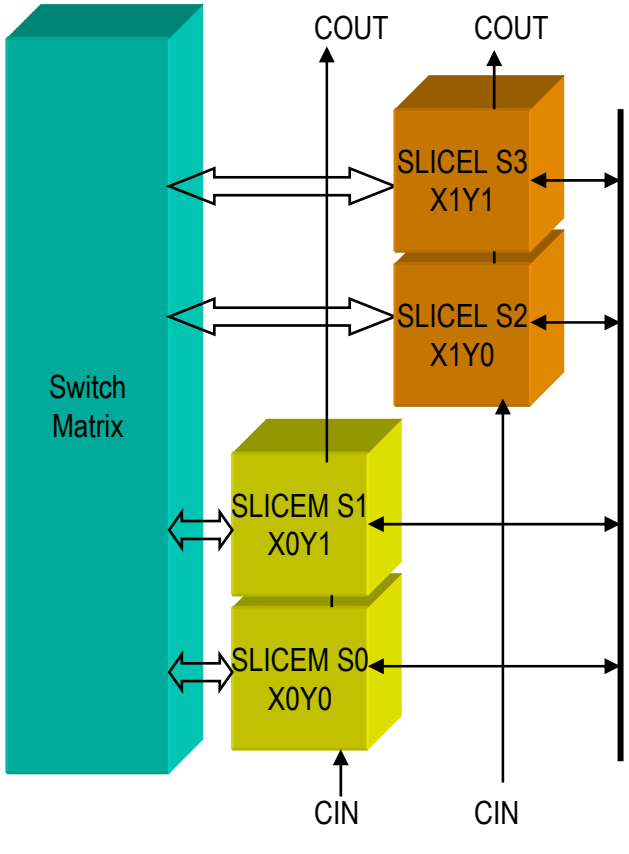
- Programmable Input Output Blocks (IOB).
- Clock Management Blocks (DCM).
- Configurable Logic Blocks (CLB).
- Flexible Synchronous Memory (BlockRAM).
- A variety of programmable routing resources.

Slices and CLBs

- Each Spartan 3 CLB contains four slices
  - Local routing provides feedback between slices in the same CLB, and it provides routing to neighboring CLBs
  - A switch matrix provides access to general routing resources



Slices and CLBs



- Four slices per CLB.
  - 2 SLICEL are Logic only.
  - 2 SLICEM are Logic / Memory.
- Fast arithmetic functions with cascadable look-ahead carry chains.

Spartan-3 Slice Capabilities

- Basic SLICEL structure of a slice is two 4-input look-up tables followed by two D flip-flops (plus extra stuff).
- Basic SLICEM structure is like SLICEL but the LUT4s may instead be used as RAM or a shift register.

SLICEM	Function	SLICEL
✓	Logic/ROM	✓
✓	Arithmetic/Carry	✓
✓	Wide Mux	✓
✓	Distributed RAM	
✓	Shift Register	

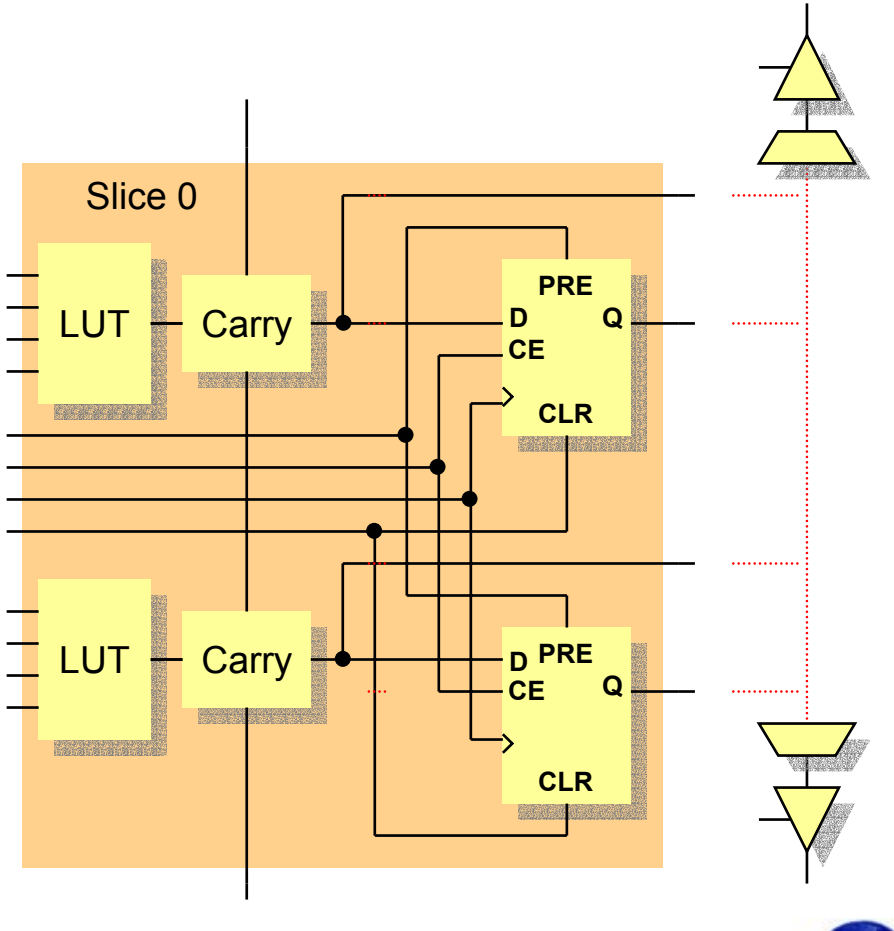
Simplified Slice Structure

Each slice has four outputs

- Two registered outputs, two non-registered outputs
- Two BUFTs associated with each CLB, accessible by all 16 CLB outputs

Carry logic runs vertically, up only

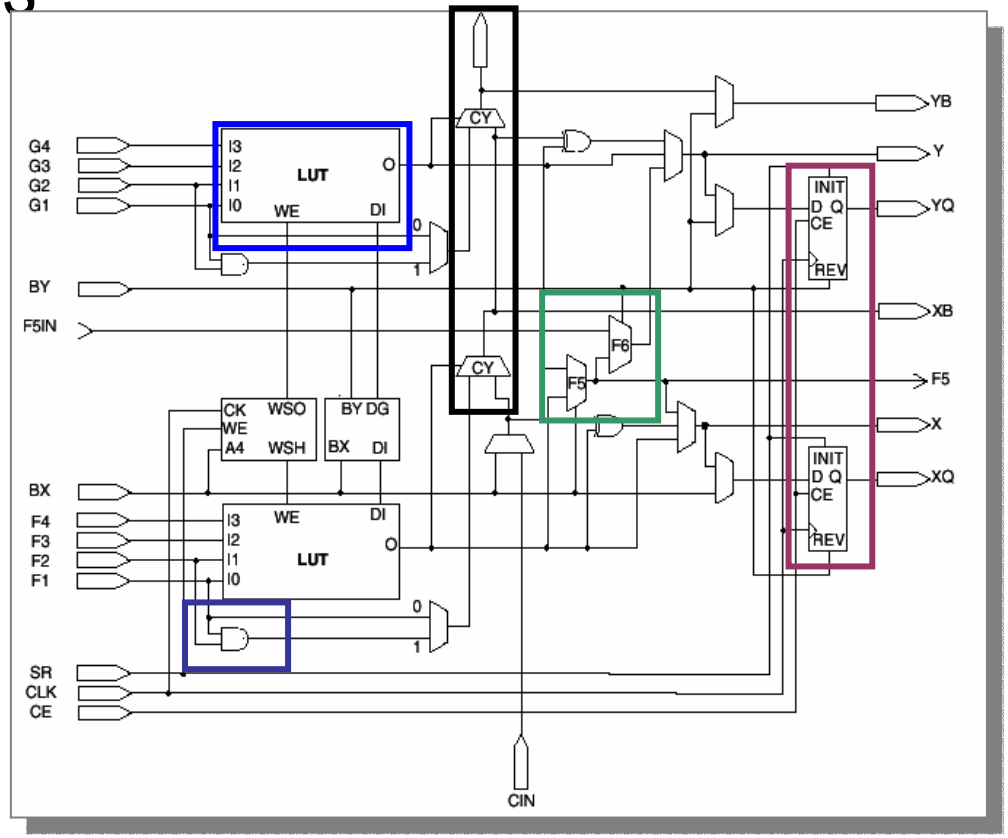
- Two independent carry chains per CLB



Detailed Slice Structure

The next few slides discuss the slice features

- LUTs
- MUXF5, MUXF6, MUXF7, MUXF8 (only the F5 and F6 MUX are shown in this diagram)
- Carry Logic
- MULT_ANDs
- Sequential Elements

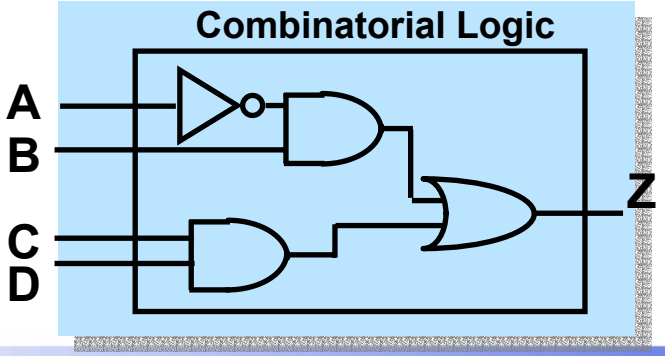


Look-Up Tables

Combinatorial logic is stored in Look-Up Tables (LUTs)

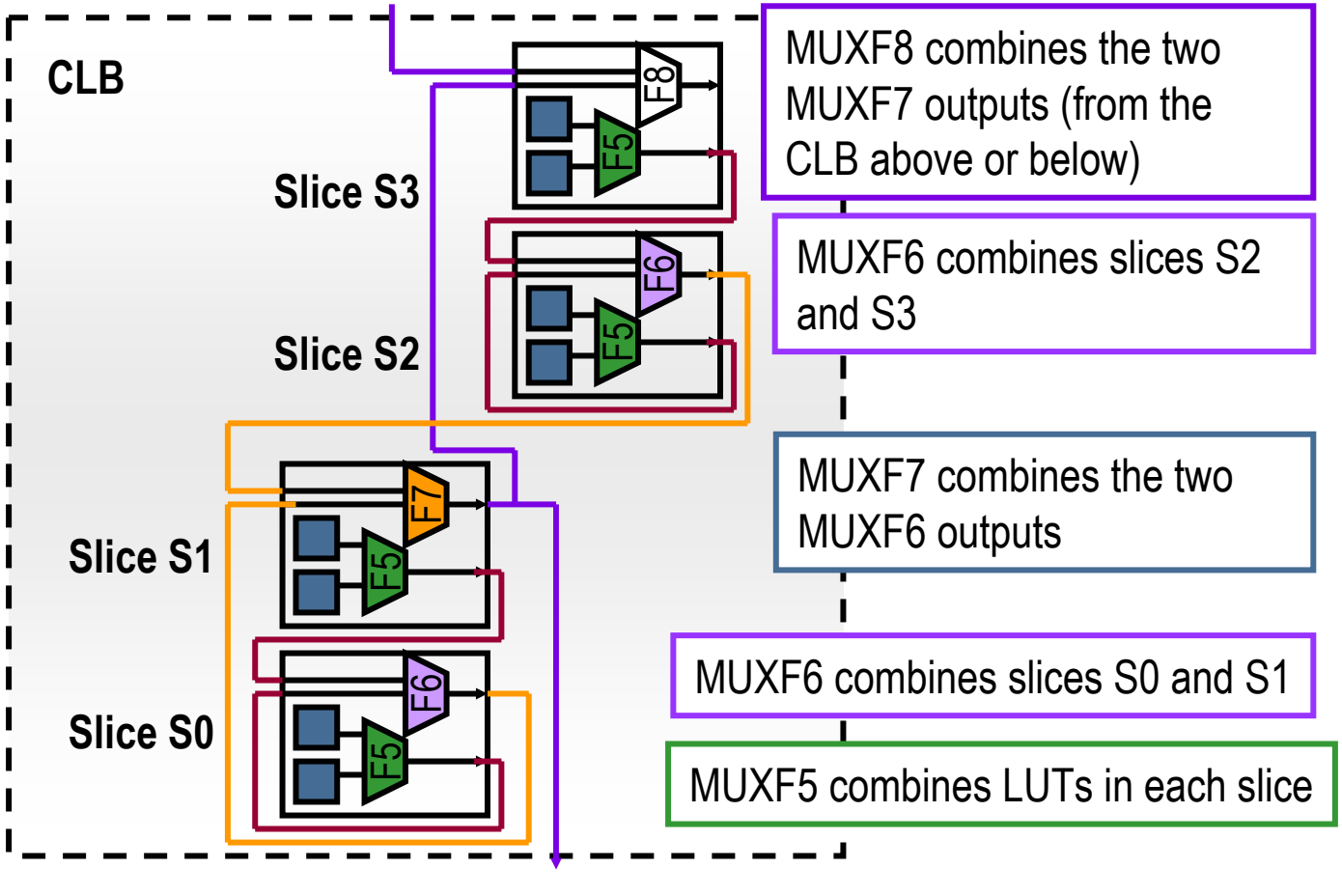
- Also called Function Generators (FGs)
- Capacity is limited by the number of inputs, not by the complexity
- Cascaded for wide-input functions

Delay through the LUT is constant



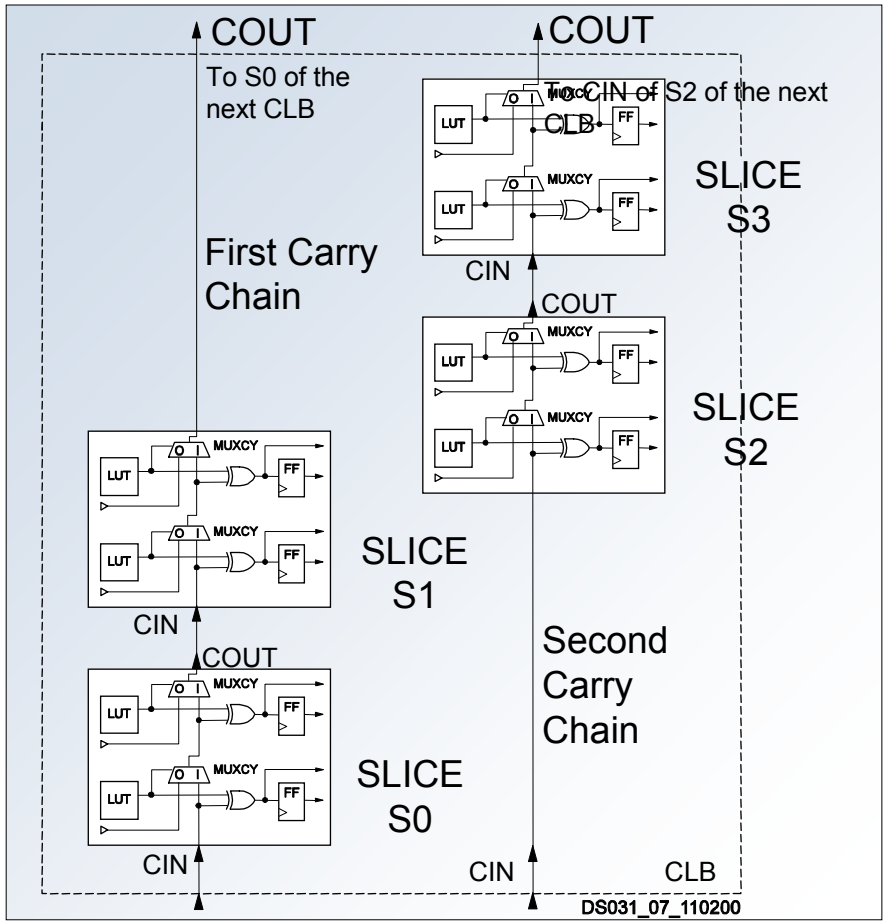
A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Connecting Look-Up Tables Dedicated Multiplexers



Fast Carry Logic

- Simple, fast, and complete arithmetic Logic
  - Dedicated XOR gate for single-level sum completion
  - Uses dedicated routing resources
  - All synthesis tools can infer carry logic



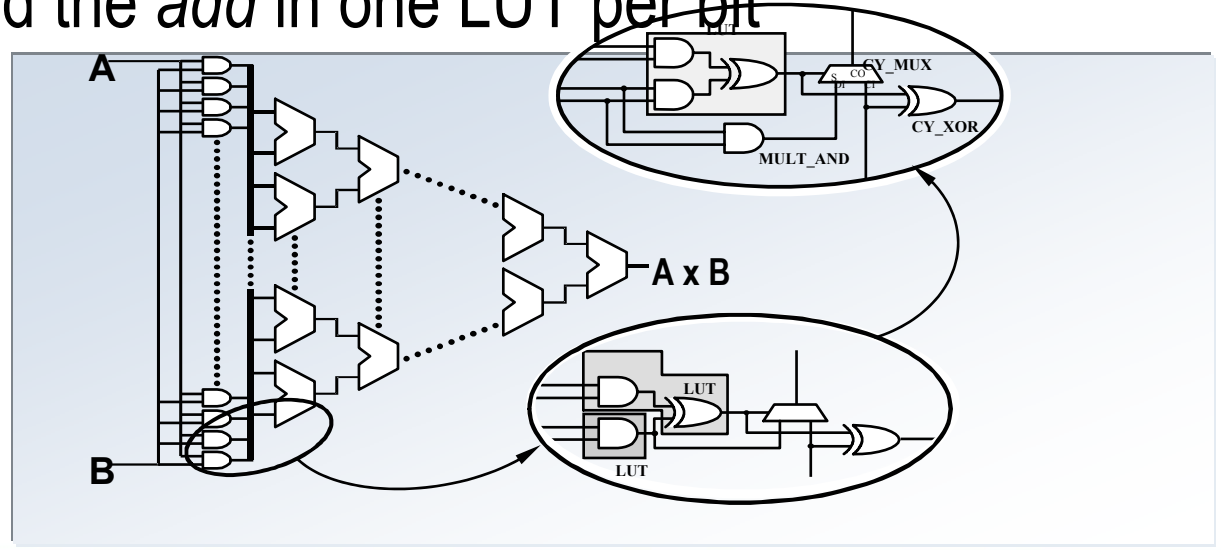
Arithmetic / Carry Logic

- Dedicated look-ahead carry logic.
  - High performance for counters and arithmetic functions.
  - Can be used to cascade LUTs for wide-input logic functions.
- Resources for efficient LUT implementation of shift and add multipliers.

MULT_AND Gate

Highly efficient multiply and add implementation

- Earlier FPGA architectures require two LUTs per bit to perform the multiplication and addition
- The MULT_AND gate enables an area reduction by performing the *multiply* and the *add* in one LUT per bit



Flexible Sequential Elements

Either flip-flops or latches

Two in each slice; eight in each CLB

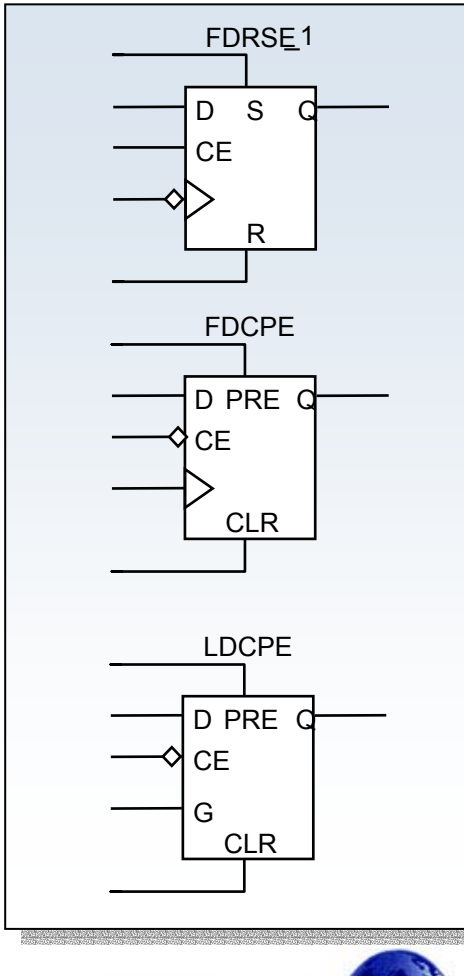
Inputs come from LUTs or from an independent CLB input

Separate set and reset controls

- Can be synchronous or asynchronous

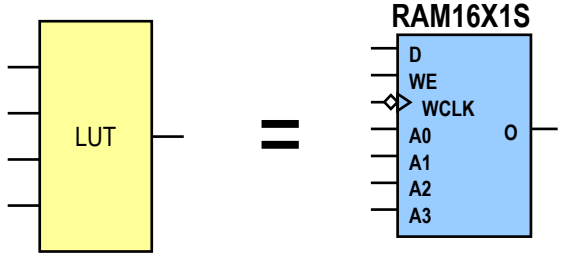
All controls are shared within a slice

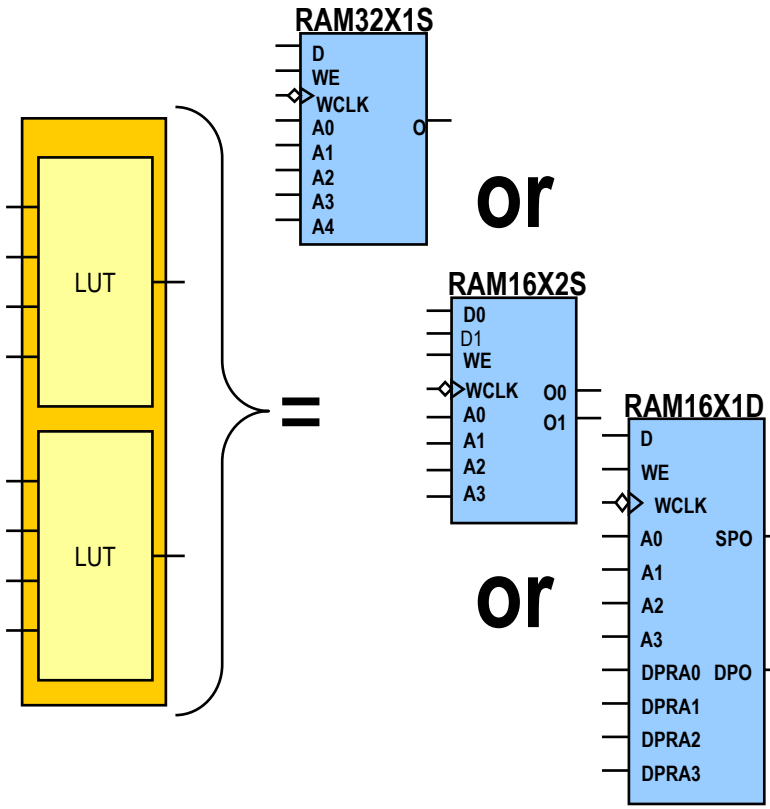
- Control signals can be inverted locally within a slice



Distributed RAM

- A LUT in a SLICEM may be configured for use as a RAM.
  - Implement single and dual port.
  - Cascade LUTs to increase size.
- Synchronous write only.
- Reads may be synchronous or asynchronous.





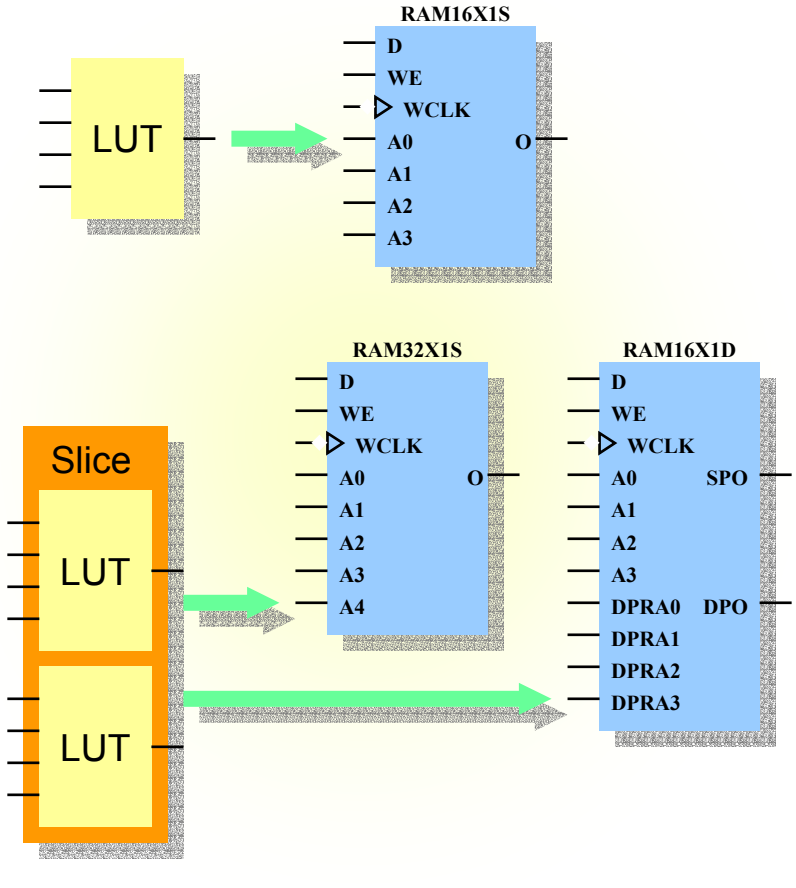
Distributed RAM

RAM and ROM are initialized during configuration

- Data can be written to RAM after configuration

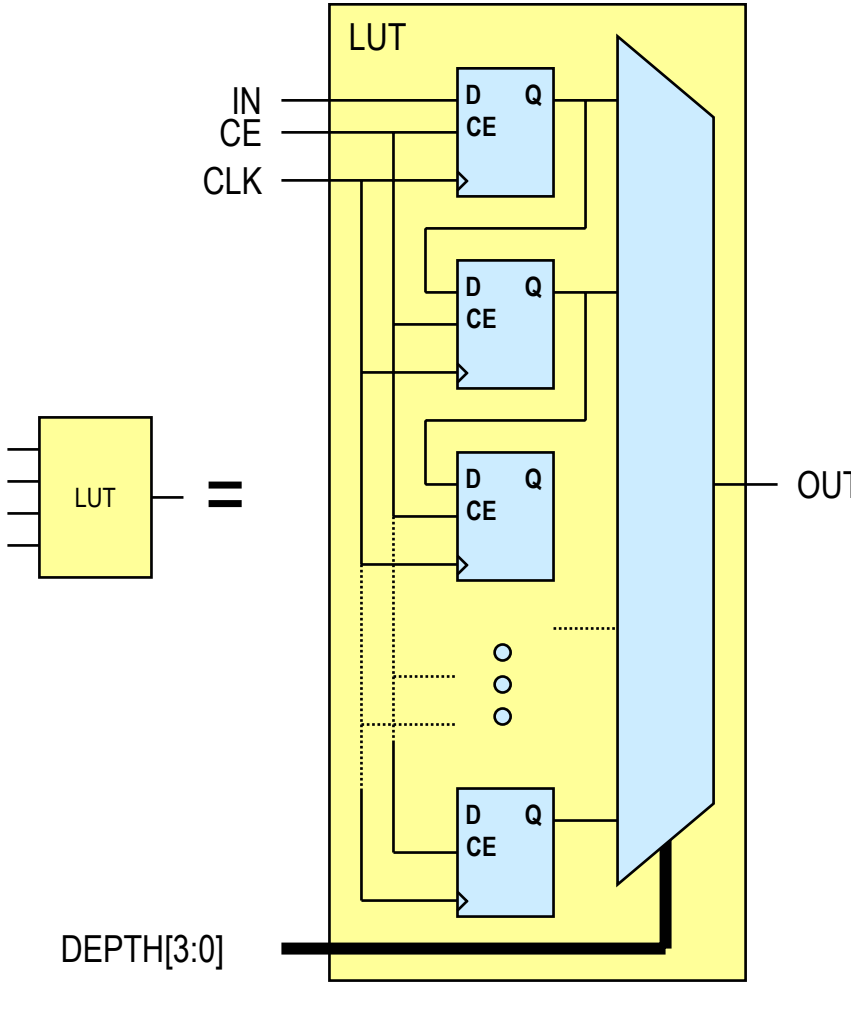
Emulated dual-port RAM

- One read/write port
- One read-only port



Shift Register LUT

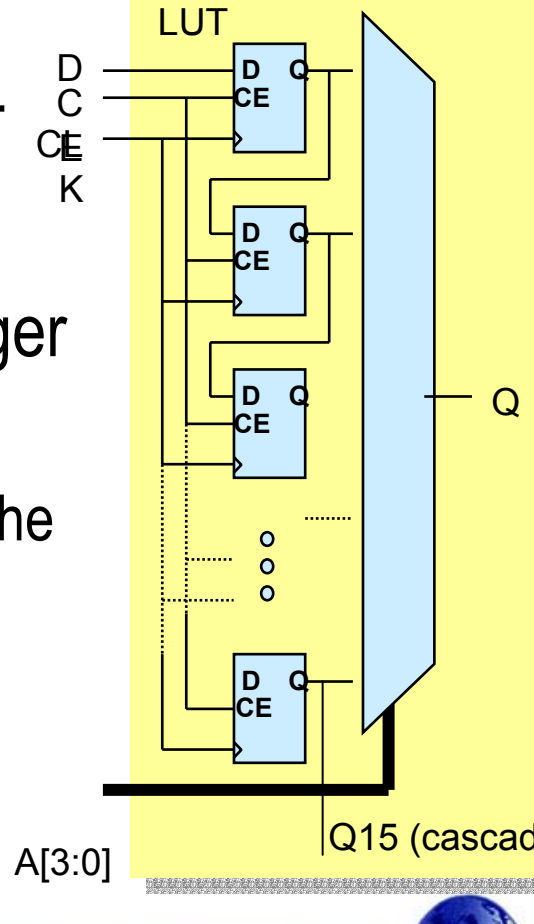
- A LUT in a SLICEM may be configured for use as a RAM.
  - Implement single and dual port.
  - Cascade LUTs to increase size.
  - Dynamically addressable delay up to 16 cycles.



Shift Register LUT

Dynamically addressable serial shift registers

- Maximum delay of 16 clock cycles per LUT (128 per CLB)
- Cascadable to other LUTs or CLBs for longer shift registers
  - Dedicated connection from Q15 to D input of the next SRL16CE
- Shift register length can be changed asynchronously by toggling address A



Spartan-3 CLB Summary

Flexible Configurable Logic Block (CLB).

- Logic, Flip Flops.
- Distributed RAM, Shift Registers.

CLB configurable for simple to complex logic.

- Any 6 input function into one logic level.

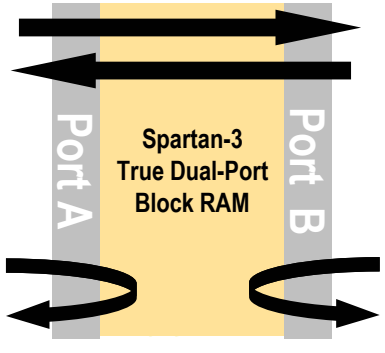
Excellent for fast arithmetic operations.

- Specialized carry logic for arithmetic operations.
- Fast DSP functions, FIR filters.

Xilinx Spartan-3 Family

- Programmable Input Output Blocks (IOB).
- Clock Management Blocks (DCM).
- Configurable Logic Blocks (CLB).
- Flexible Synchronous Memory (BlockRAM).
- A variety of programmable routing resources.

BlockRAM



- Dedicated blocks of 18-kilobit synchronous RAM.
- Ideal for many memory requirements.
- Builds both single and true dual-port memories, true dual port ideal for asynchronous FIFOs.
- May be initialized and used as synchronous ROM.

BlockRAM

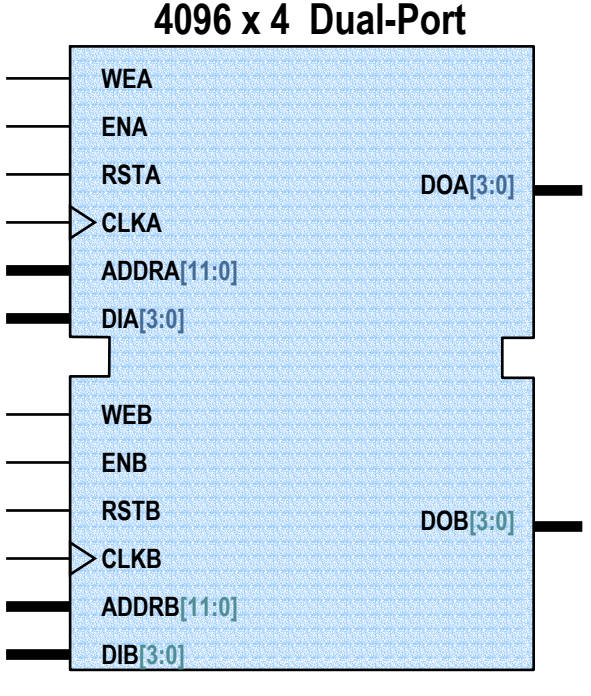
High Performance Sync Dual-Port™ RAM

- Independent configuration for port A and for port B.
- Enables data width conversion.

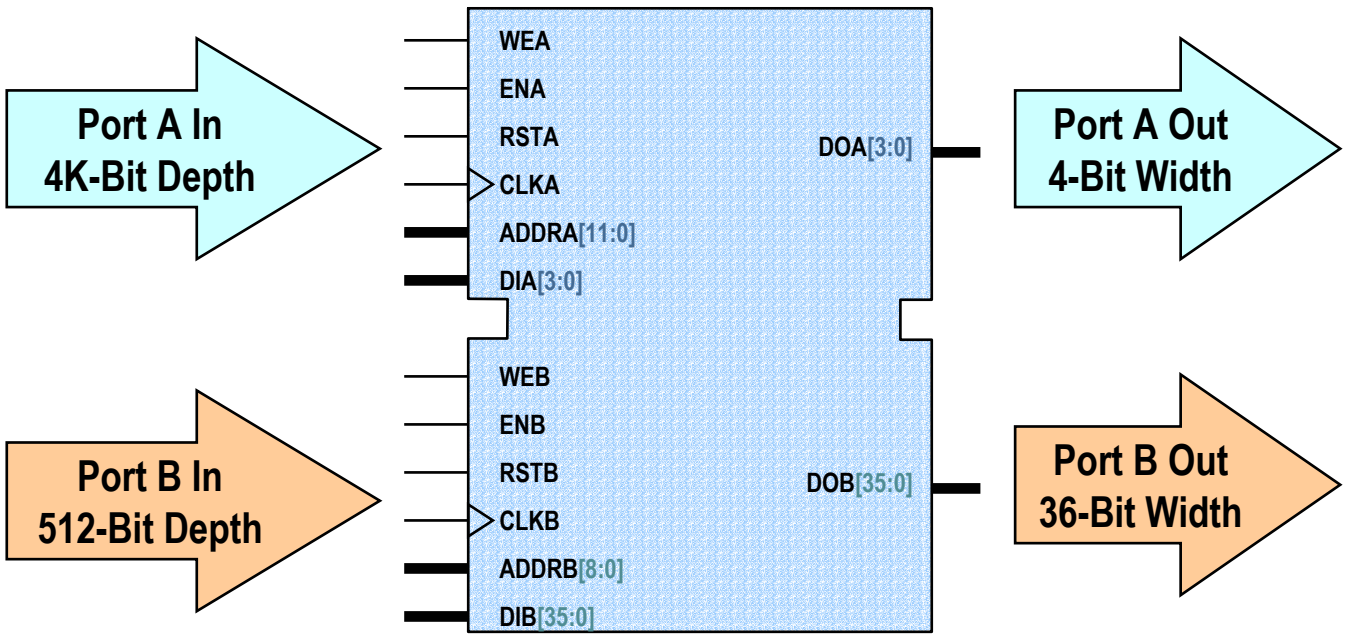
Configuration	Depth	Data bits	Parity bits
16K x 1	16Kb	1	0
8K x 2	8Kb	2	0
4K x 4	4Kb	4	0
2K x 9	2Kb	8	1
1K x 18	1Kb	16	2
512 x 36	512	32	4

True Dual-Port

- True simultaneous read and/or write to both ports.
- Each port has independent controls.
  - Address
  - Clock/Enable
  - Data
  - Read/Write
  - Reset
- May be used as two independent half-sized single port memories.



Dual-Port Flexibility

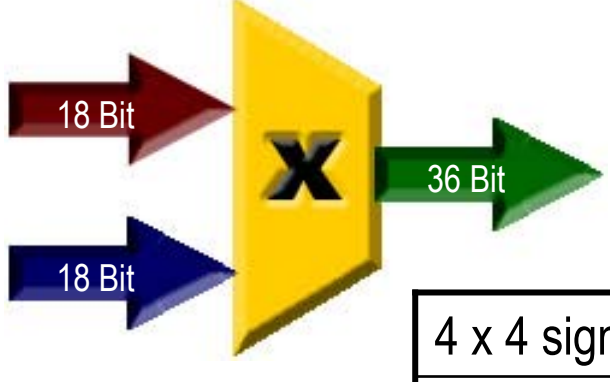


- Each port can be configured with different data width.
- Provides easy data width conversion.

Embedded Multipliers

Not actually located in CLB, but this seems a good place to bring it up…

- 18 x 18 bit signed operation.
- 17 x 17 bit unsigned operation.
- 2's complement operation.
- Combinational and pipelined options.
- Multipliers are physically located next to block SelectRAM™ memory
- Optimized to implement Multiply and Accumulate functions



4 x 4 signed
8 x 8 signed
12 x 12 signed
18 x 18 signed

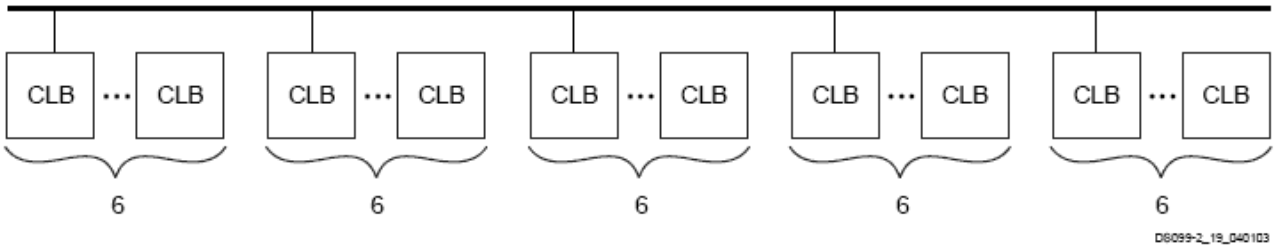
Embedded Memory Summary

- Flexible BlockRAMs enable:
  - Single and True Dual-Port RAMs.
  - FIFOs for buffering data.
  - Data width conversion.
  - Caches and register banks.

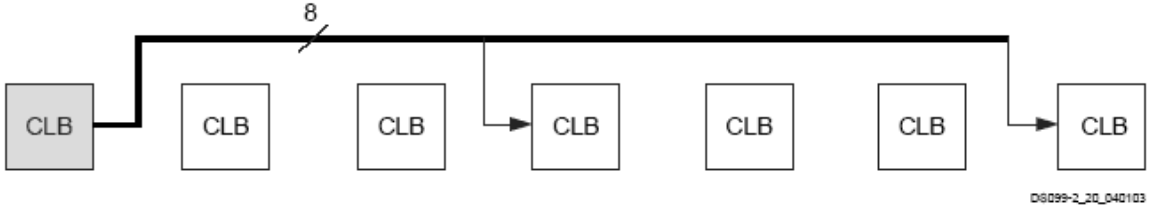
Xilinx Spartan-3 Family

- Programmable Input Output Blocks (IOB).
- Clock Management Blocks (DCM).
- Configurable Logic Blocks (CLB).
- Flexible Synchronous Memory (BlockRAM).
- A variety of programmable routing resources.

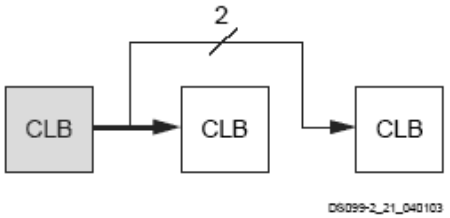
Routing Wire Types



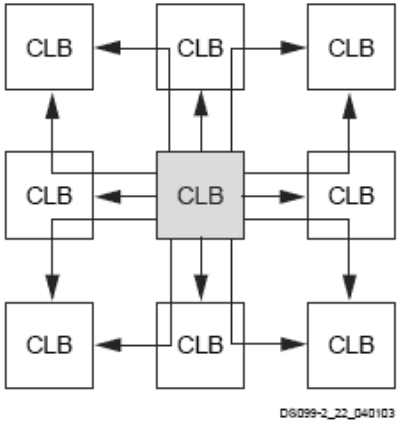
(a) Long Line



(b) Hex Line



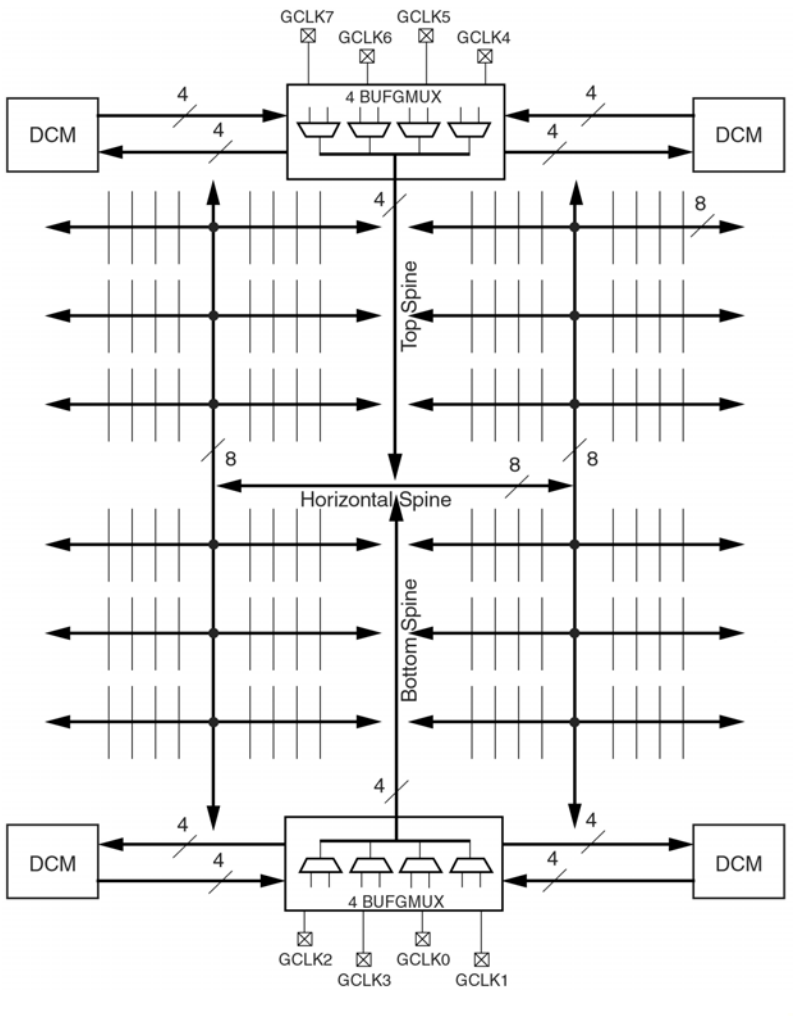
(c) Double Line



(d) Direct Lines

Global Routing

- Distribute clocks and other high fanout signals throughout the device with minimum skew.
- Eight global clock nets designed to distribute high fanout clock signals.



Routing Summary

- Vector-based routing provides predictable routing delays independent of:
  - Design placement.
  - Device size.
- Superior routing results in quick routing times and increased design performance.