practica

- entity contadorTop is
- Port (clk : in STD_LOGIC;
- rst : in STD_LOGIC;
- led : out STD_LOGIC_VECTOR (7 downto 0));
- end contadorTop;

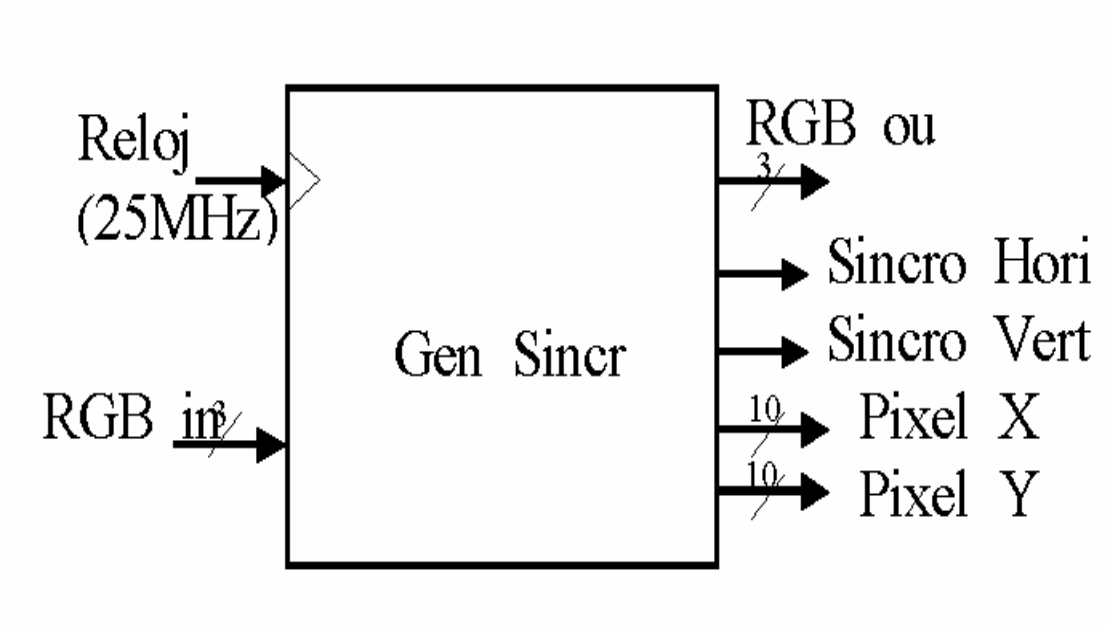
decodificador

```
PORT_DECORER: process( clk50MHz )
begin
    if( rising_edge(clk50MHz) )then
            if( write_strobe = '1' )then
              if( port_id = leds_w_port )then
                        led_register <= out_port;
              end if;
            end if;
    end if;
end process;

constant leds_w_port : std_logic_vector( 7 downto 0 ) := x"00";
signal led_register             : std_logic_vector( 7 downto 0 ) := x"00";

led <= led_register;
```

Vga driver


Reloj
(25MHz)
RGB in
3
Gen Sincr
RGB ou
3
Sincro Hori
Sincro Vert
10
Pixel X
10
Pixel Y

SincronismoHorizontal

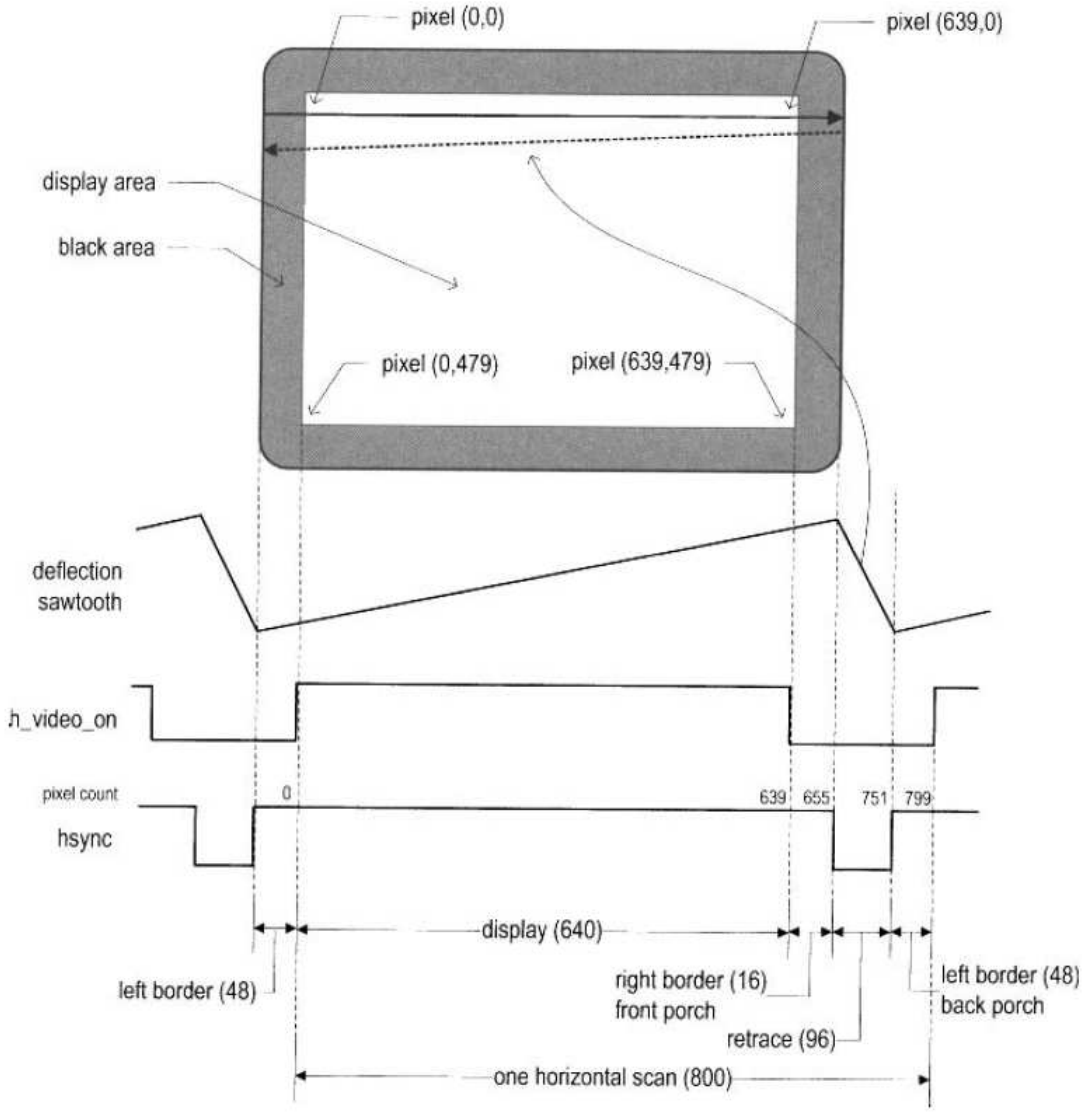


Figure 12.4 Timing diagram of a horizontal scan.

Sincronismo Vertical

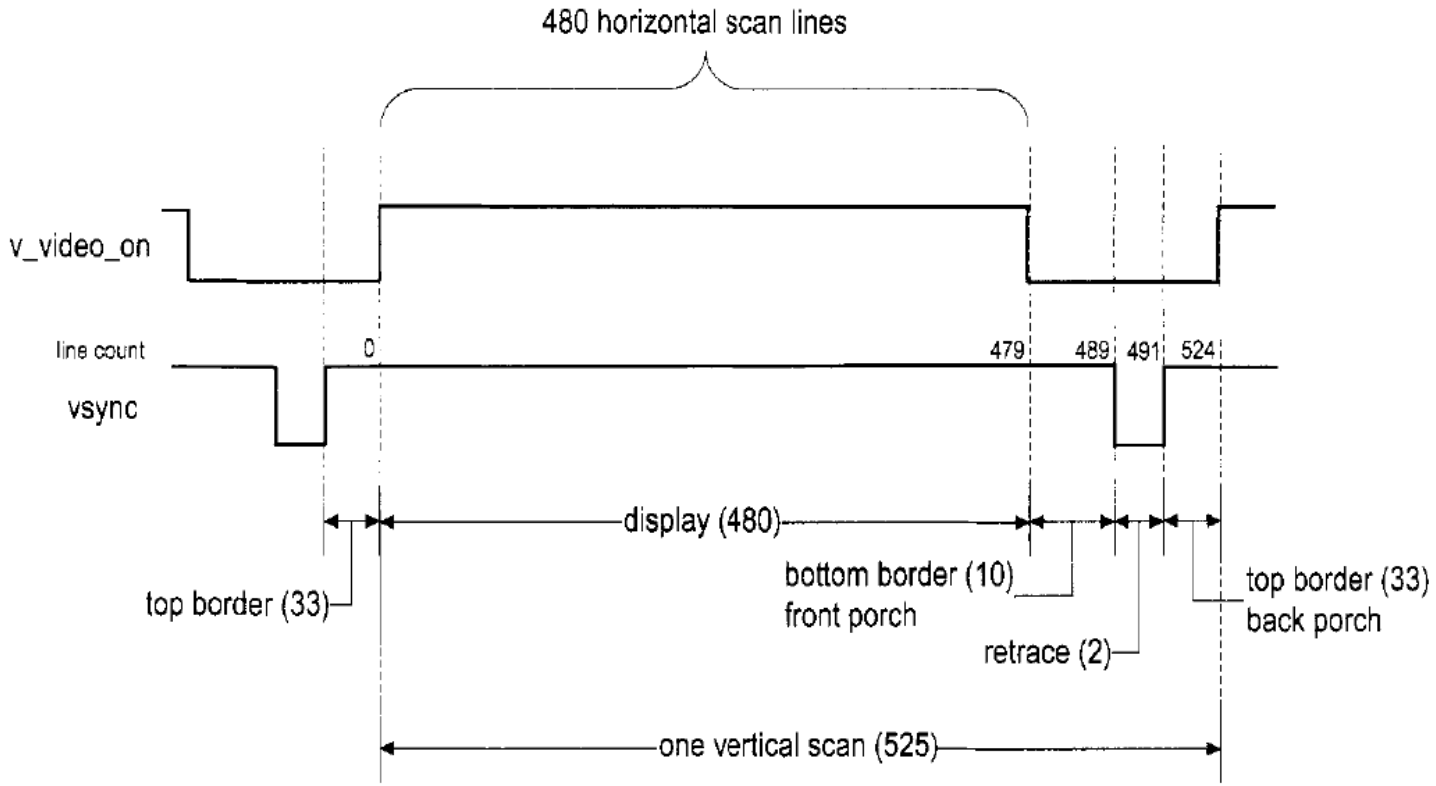


Figure 12.5 Timing diagram of a vertical scan.